Reference Hardware Design Guideline

USB Board

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1.0	May 25, 2020

Panasonic Corporation

Automotive Company R&D Division

Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

Reference Documents

No.	Document Filename	Ver.	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

Contents

Figures and Tables

1. USB Board

USB Board is connected to Control Board and mainly enables USB communication between external units. Three channels of USB3.0 Super-Speed, which may vary according to SoC, is connected as interface with SoC.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

1.1. Board Outline

The following figure shows USB Board dimension. 1.2[mm] is the assumed thickness, but if the design modification is required, special attention should be paid to avoid the interference with other boards.

The interface to Control Board is a 60-pin board-to-board connector mounted on the solder side of USB Board. The external interface connectors are mounted on the component side so as to avoid the interference with another board when assembled.

The spacing between the board and chassis is shown as below. The chassis is also an important factor to be considered when determining the position of an external interface.

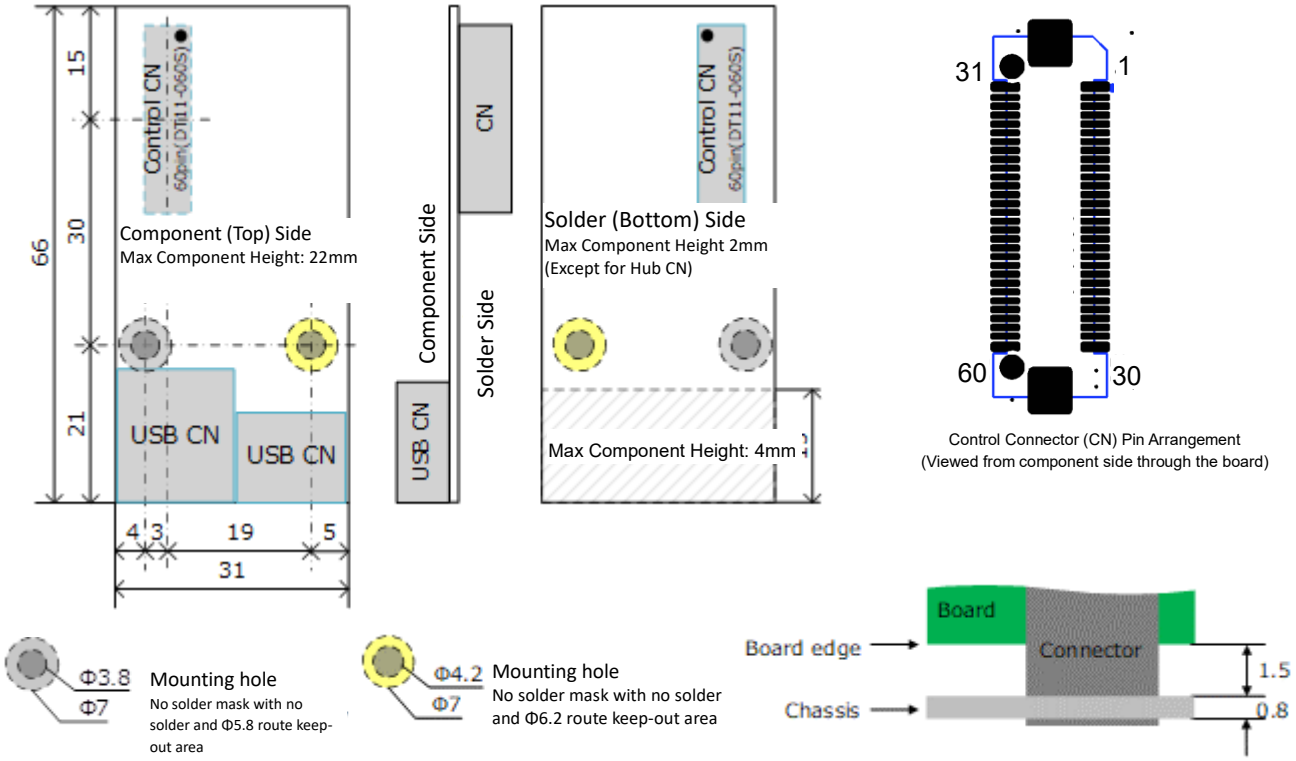


Figure 1 Board Dimension

When there is not enough space in USB Board, Space in VideoIn3 Board can be used to increase more area on USB Board as needed. In such case, the board will no longer function as VideoOut3 Board.

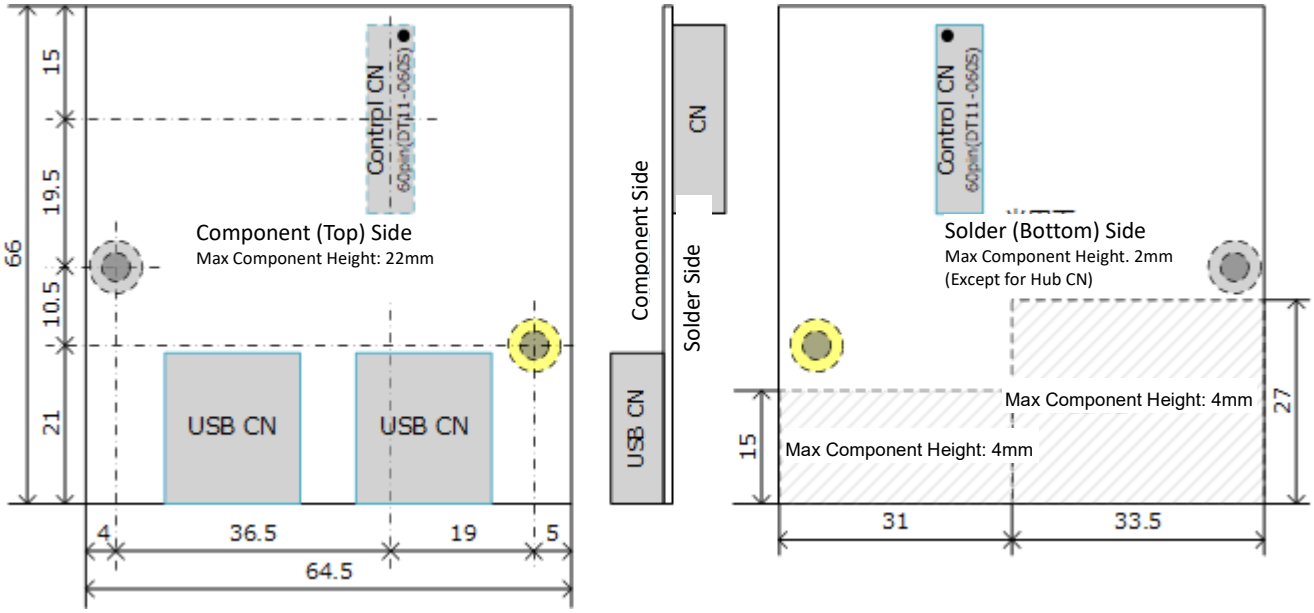


Figure 2 Expanded Board Dimension

1.2. Power Supply

There is five power supply rails that power USB Board. The specification of each power is shown in Table 1.

Table 1 USB Board Power Supply

Signal Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
+B_VPH		12		1200	Pin 28, Pin29, Pin30 (3 pins)
VDD_5P8V		5.87		1000	Pin 58, Pin 59, Pin 60 (3pins)
VDD_3P3V		3.3		200	Pin 27 (1 pin)
VDD_USB_1P8V		1.8		200	Pin 57 (1 pin)
VDD_USB_CORE		1.2		200	Pin 56 (1 pin)

A power circuit can be built on USB Board if no power source is available for an intended purpose.

Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, one of the possible solutions is to use another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards). Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins.

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

1.3. Board-to-Board Interface

60-pin board-to-board connectors is used to connect Control Board to USB Board. A receptacle connector is assumed to be used on the side of Control board and (KEL DT01-060S), and a plug connector (KEL DT11-060S-10) is assumed to be used on the side of USB board.

These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of ±0.5 [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA].

The voltage for signals interfacing with Control Board should be able to adjust to both 1.8[V] and 3.3[V] as USB Board and Ethernet Board uses signals of the same terminal voltage. The voltage level should be able to shift using such as a level shifter to make the voltage for signals consistent. When a signal output is on USB Board side and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.

A pull-up or pull-down resistor should be added to USB Board for the external resistor required for I2C signal, etc.

1.3.1. USB Board Interface (R-Car H3 Reference Hardware)

Figure 3 and Figure 4 show schematics illustrating the connection between Control Board and USB Board for R-Car H3 Reference Hardware. Pin assignments of the connector (USB CN) and the connected terminals are listed on Table 2.

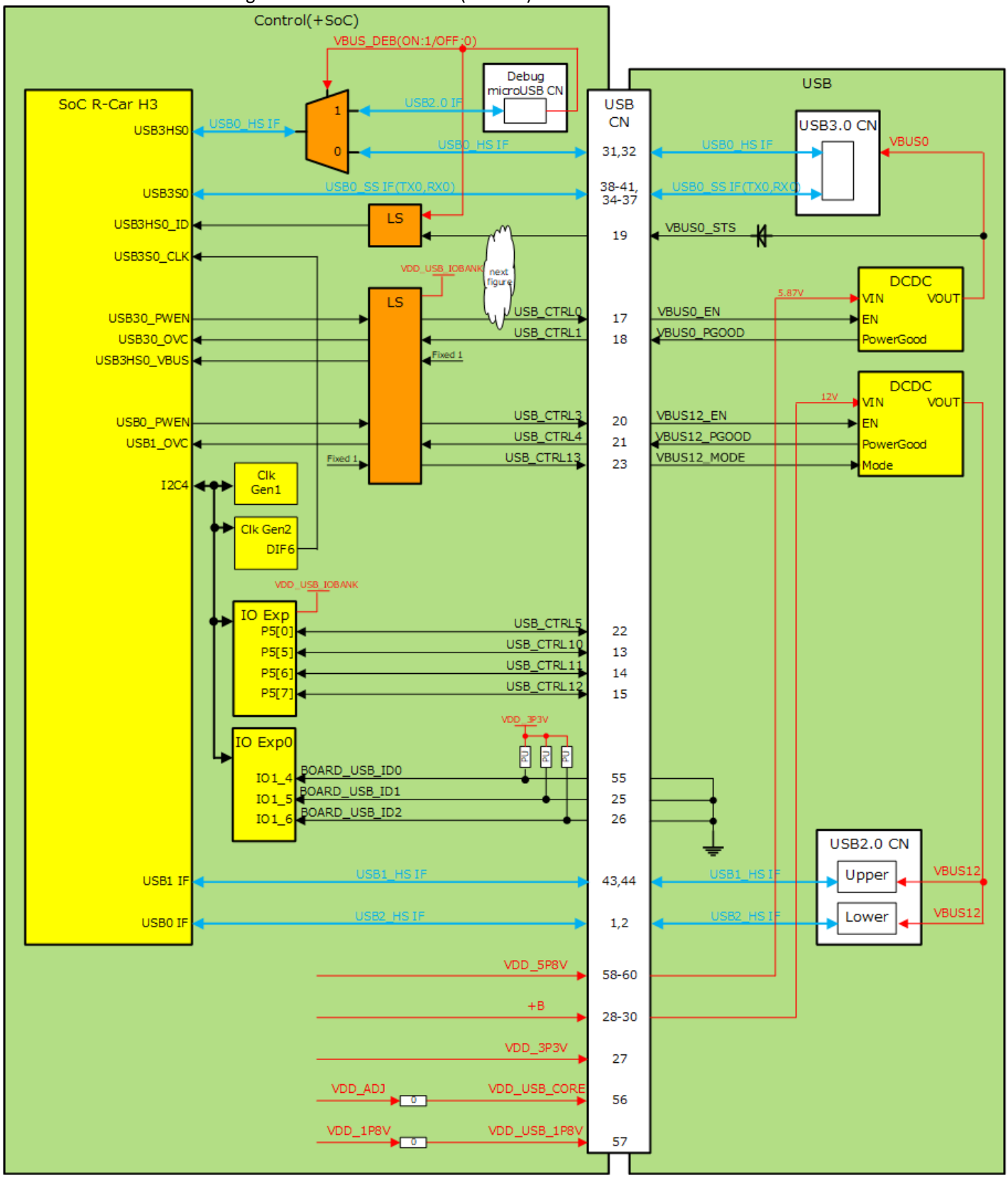


Figure 3 Connectivity between USB Board and Control Board (R-Car H3 Reference Hardware)

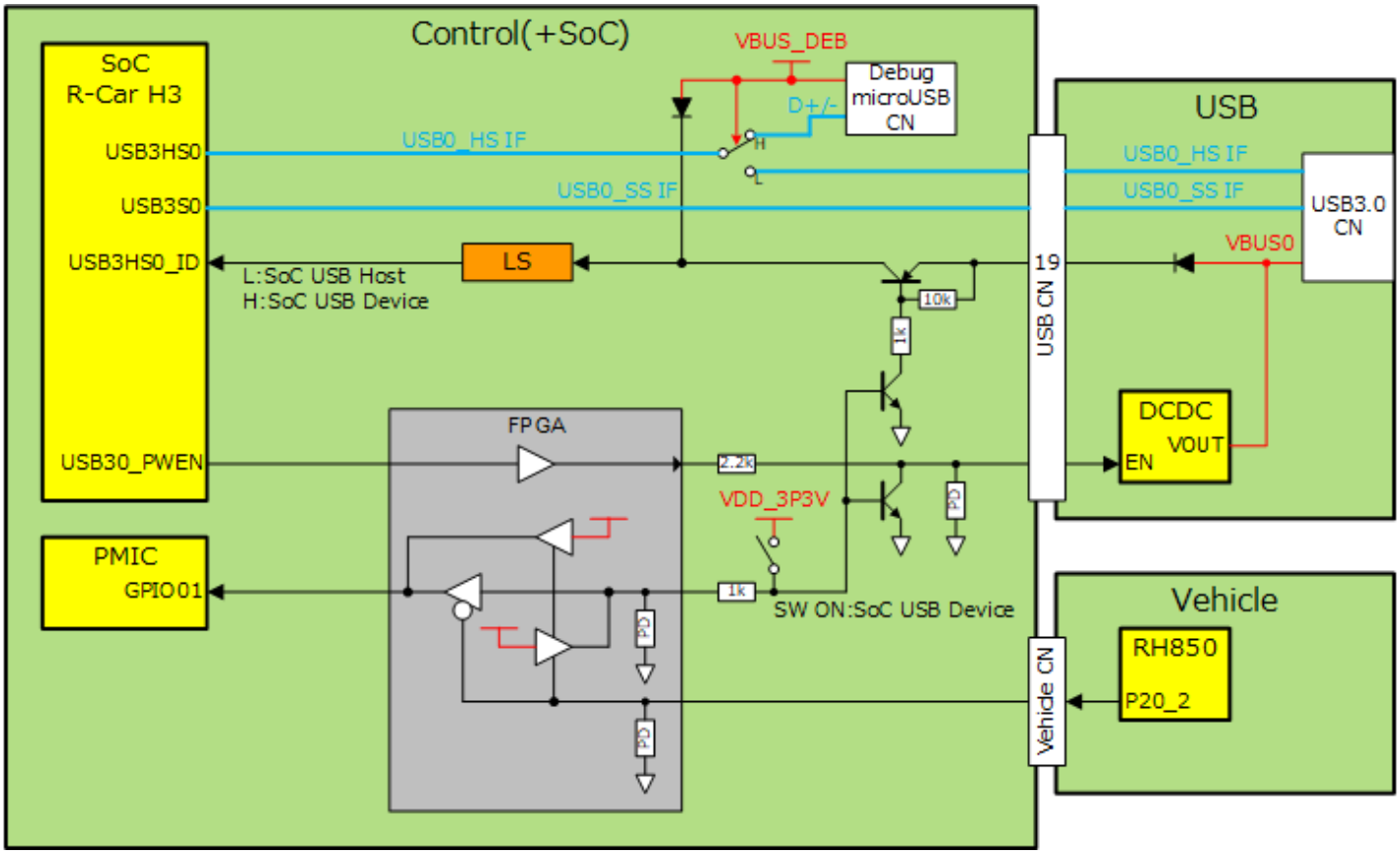


Figure 4 USB Debugging Schematic (R-Car H3 Reference Hardware)

Table 2 Connector (USB CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description
32	USB0_D_P	<>	LVDS	R-Car H3 "USB3HS0_DP" pin	USB3 ch0 HS Data+
31	USB0_D_M	<>	LVDS	R-Car H3 "USB3HS0_DM" pin	USB3 ch0 HS Data-
38	USB0_SS_TX0_P	>	LVDS	R-Car H3 "USB3S0_TX_P" pin	USB3 ch0 SS Tx(SoC Tx) Data+
39	USB0_SS_TX0_M	>	LVDS	R-Car H3 "USB3S0_TX_M" pin	USB3 ch0 SS Tx(SoC Tx) Data-
40	USB0_SS_RX0_P	<	LVDS	R-Car H3 "USB3S0_RX_P" pin	USB3 ch0 SS Rx(SoC Rx) Data+
41	USB0_SS_RX0_M	<	LVDS	R-Car H3 "USB3S0_RX_M" pin	USB3 ch0 SS Rx(SoC Rx) Data-
34	USB0_SS_TX1_P	-	-	NC	-
35	USB0_SS_TX1_M	-	-	NC	-
36	USB0_SS_RX1_P	-	-	NC	-
37	USB0_SS_RX1_M	-	-	NC	-
44	USB1_D_P	<>	LVDS	R-Car H3 "DP1" pin	USB2 ch1 HS Data+
43	USB1_D_M	<>	LVDS	R-Car H3 "DM1" pin	USB2 ch1 HS Data-
50	USB1_SS_TX0_P	-	-	NC	-
51	USB1_SS_TX0_M	-	-	NC	-
52	USB1_SS_RX0_P	-	-	NC	-
53	USB1_SS_RX0_M	-	-	NC	-
46	USB1_SS_TX1_P	-	-	NC	-
47	USB1_SS_TX1_M	-	-	NC	-
48	USB1_SS_RX1_P	-	-	NC	-
49	USB1_SS_RX1_M	-	-	NC	-
2	USB2_D_P	<>	LVDS	R-Car H3 "DP0" pin	USB2 ch0 HS Data+
1	USB2_D_M	<>	LVDS	R-Car H3 "DM0" pin	USB2 ch0 HS Data-
4	USB2_SS_TX0_P	-	-	NC	-
5	USB2_SS_TX0_M	-	-	NC	-
6	USB2_SS_RX0_P	-	-	NC	-
7	USB2_SS_RX0_M	-	-	NC	-
17	USB_CTRL0	>	3.3[V] *1	R-Car H3 "USB30_PWEN" pin	USB3 ch0 VBUS Enable (H:ON)
18	USB_CTRL1	<	3.3[V] *1	R-Car H3 "USB30_OVC" pin	USB3 ch0 VBUS PowerGood (L:Fault)

Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description
20	USB_CTRL3	>	3.3[V] *1	R-Car H3 "USB0_PWEN" pin	USB2 ch0,1 VBUS Enable (H:ON)
21	USB_CTRL4	<	3.3[V] *1	R-Car H3 "USB1_OVC" pin	USB2 ch0,1 VBUS PowerGood (H:Good)
22	USB_CTRL5	<>	3.3[V] *1	IO Expander-5 bit0	No used
9	USB_CTRL6	-	-	No used	-
10	USB_CTRL7	-	-	No used	-
11	USB_CTRL8	-	-	No used	-
12	USB_CTRL9	-	-	No used	-
13	USB_CTRL10	<>	3.3[V] *1	IO Expander-5 bit5	No used
14	USB_CTRL11	<>	3.3[V] *1	IO Expander-5 bit6	No used
15	USB_CTRL12	<>	3.3[V] *1	IO Expander-5 bit7	No used
23	USB_CTRL13	>	3.3[V] *2	Fixed High	USB2 ch0,1 VBUS Mode (H:Force PWM)
19	VBUS0_STS	<	5.0[V]	R-Car H3 "USB3HS0_ID" pin	USB3 ch0 VBUS
55	BOARD_USB_ID0	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_4" pin, Pull-up	USB Board ID bit0
25	BOARD_USB_ID1	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_5" pin, Pull-up	USB Board ID bit1
26	BOARD_USB_ID2	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_6" pin, Pull-up	USB Board ID bit2
28	+B_VPH	>	Power:12[V]	Power connector	Power
29	+B_VPH	>	Power:12[V]	Power connector	Power
30	+B_VPH	>	Power:12[V]	Power connector	Power
58	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
59	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
60	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
27	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
57	VDD_USB_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
56	VDD_USB_CORE	>	Power:1.2[V]	1.2[V] output LDO	Power
3	GND	-	GND	GND	GND
8	GND	-	GND	GND	GND
16	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
33	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description
42	GND	-	GND	GND	GND
45	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND

*1: Voltage depends on the power supply switch setting (FPGA USB IO voltage) on Control Board
*2: Voltage depends on Vehicle Board (IO_VEHICLE voltage)

1.3.2. USB board Interface (Standard Reference Hardware)

Figure 5 shows the schematic of Control Board with USB CN that connects to USB Board for Standard Reference Hardware. Pin assignments of the connector (USB CN) and the connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

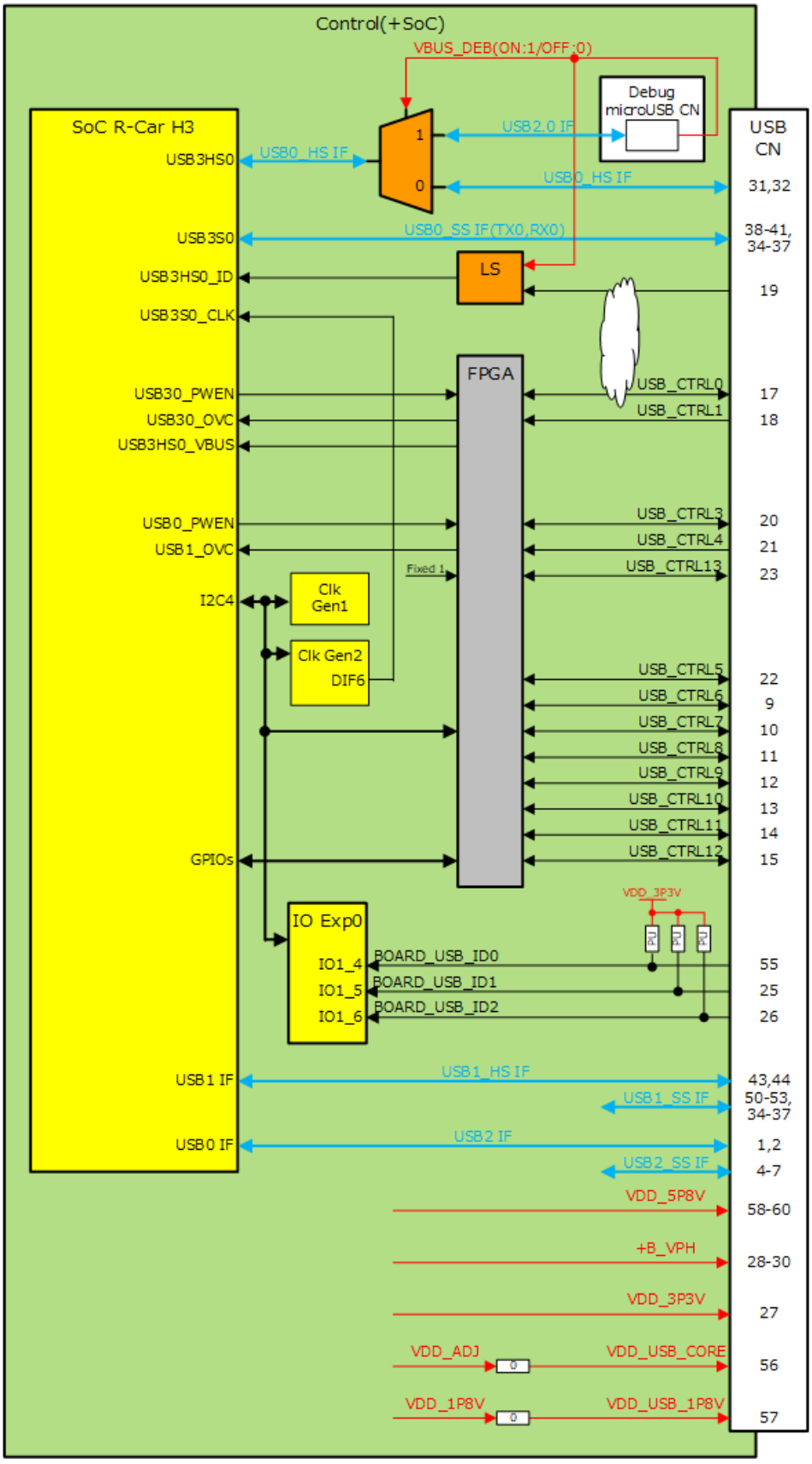


Figure 5 Connectivity between USB Board and Control Board (Standard Reference Hardware)

Table 3 Connector (USB CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description Example of use
32	USB0_D_P	<>	LVDS	SoC USB3.0 ch0 HS Data+	USB3.0 ch0 HS Data+
31	USB0_D_M	<>	LVDS	SoC USB3.0 ch0 HS Data-	USB3.0 ch0 HS Data-
38	USB0_SS_TX0_P	>	LVDS	SoC USB3.0 ch0 SS Tx0 Data+(SoC Tx)	USB3.0 ch0 SS Tx0 Data+(SoC Tx)
39	USB0_SS_TX0_M	>	LVDS	SoC USB3.0 ch0 SS Tx0 Data-(SoC Tx)	USB3.0 ch0 SS Tx0 Data-(SoC Tx)
40	USB0_SS_RX0_P	<	LVDS	SoC USB3.0 ch0 SS Rx0 Data+(SoC Rx)	USB3.0 ch0 SS Rx0 Data+(SoC Rx)
41	USB0_SS_RX0_M	<	LVDS	SoC USB3.0 ch0 SS Rx0 Data-(SoC Rx)	USB3.0 ch0 SS Rx0 Data-(SoC Rx)
34	USB0_SS_TX1_P	>	LVDS	SoC USB3.0 ch0 SS Tx1 Data+(SoC Tx)	NC, USB3.0 ch0 SS Tx1 Data+(SoC Tx)
35	USB0_SS_TX1_M	>	LVDS	SoC USB3.0 ch0 SS Tx1 Data-(SoC Tx)	NC, USB3.0 ch0 SS Tx1 Data-(SoC Tx)
36	USB0_SS_RX1_P	<	LVDS	SoC USB3.0 ch0 SS Rx1 Data+(SoC Rx)	NC, USB3.0 ch0 SS Rx1 Data+(SoC Rx)
37	USB0_SS_RX1_M	<	LVDS	SoC USB3.0 ch0 SS Rx1 Data-(SoC Rx)	NC, USB3.0 ch0 SS Rx1 Data-(SoC Rx)
44	USB1_D_P	<>	LVDS	SoC USB3.0 ch1 HS Data+	USB3.0 ch1 HS Data+
43	USB1_D_M	<>	LVDS	SoC USB3.0 ch1 HS Data-	USB3.0 ch1 HS Data-
50	USB1_SS_TX0_P	>	LVDS	SoC USB3.0 ch1 SS Tx0 Data+(SoC Tx)	NC, USB3.0 ch1 SS Tx0 Data+(SoC Tx)
51	USB1_SS_TX0_M	>	LVDS	SoC USB3.0 ch1 SS Tx0 Data-(SoC Tx)	NC, USB3.0 ch1 SS Tx0 Data-(SoC Tx)
52	USB1_SS_RX0_P	<	LVDS	SoC USB3.0 ch1 SS Rx0 Data+(SoC Rx)	NC, USB3.0 ch1 SS Rx0 Data+(SoC Rx)
53	USB1_SS_RX0_M	<	LVDS	SoC USB3.0 ch1 SS Rx0 Data-(SoC Rx)	NC, USB3.0 ch1 SS Rx0 Data-(SoC Rx)
46	USB1_SS_TX1_P	>	LVDS	SoC USB3.0 ch1 SS Tx1 Data+(SoC Tx)	NC, USB3.0 ch1 SS Tx1 Data+(SoC Tx)
47	USB1_SS_TX1_M	>	LVDS	SoC USB3.0 ch1 SS Tx1 Data-(SoC Tx)	NC, USB3.0 ch1 SS Tx1 Data-(SoC Tx)
48	USB1_SS_RX1_P	<	LVDS	SoC USB3.0 ch1 SS Rx1 Data+(SoC Rx)	NC, USB3.0 ch1 SS Rx1 Data+(SoC Rx)
49	USB1_SS_RX1_M	<	LVDS	SoC USB3.0 ch1 SS Rx1 Data-(SoC Rx)	NC, USB3.0 ch1 SS Rx1 Data-(SoC Rx)
2	USB2_D_P	<>	LVDS	SoC USB3.0 ch2 HS Data+	USB3.0 ch2 HS Data+
1	USB2_D_M	<>	LVDS	SoC USB3.0 ch2 HS Data-	USB3.0 ch2 HS Data-
4	USB2_SS_TX0_P	>	LVDS	SoC USB3.0 ch2 SS Tx Data+(SoC Tx)	NC, USB3.0 ch2 SS Tx Data+(SoC Tx)
5	USB2_SS_TX0_M	>	LVDS	SoC USB3.0 ch2 SS Tx Data-(SoC Tx)	NC, USB3.0 ch2 SS Tx Data-(SoC Tx)
6	USB2_SS_RX0_P	<	LVDS	SoC USB3.0 ch2 SS Rx Data+(SoC Rx)	NC, USB3.0 ch2 SS Rx Data+(SoC Rx)
7	USB2_SS_RX0_M	<	LVDS	SoC USB3.0 ch2 SS Rx Data-(SoC Rx)	NC, USB3.0 ch2 SS Rx Data-(SoC Rx)
17	USB_CTRL0	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch0 VBUS Enable
18	USB_CTRL1	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch0 VBUS Power Status

Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description Example of use
20	USB_CTRL3	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch1 VBUS Enable
21	USB_CTRL4	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch1 VBUS Power Status
22	USB_CTRL5	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch2 VBUS Enable
9	USB_CTRL6	<>	VCCIO_FPGA	FPGA	GPIO
10	USB_CTRL7	<>	VCCIO_FPGA	FPGA	GPIO
11	USB_CTRL8	<>	VCCIO_FPGA	FPGA	GPIO
12	USB_CTRL9	<>	VCCIO_FPGA	FPGA	GPIO
13	USB_CTRL10	<>	VCCIO_FPGA	FPGA	GPIO
14	USB_CTRL11	<>	VCCIO_FPGA	FPGA	GPIO
15	USB_CTRL12	<>	VCCIO_FPGA	FPGA	GPIO
23	USB_CTRL13	<>	IO_VEHICLE	FPGA	GPIO
19	VBUS0_STS	<	5.0[V]	Refer to figure.4	USB3.0 ch0 VBUS
55	BOARD_USB_ID0	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_4" pin, Pull-up	USB Board ID bit0
25	BOARD_USB_ID1	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_5" pin, Pull-up	USB Board ID bit1
26	BOARD_USB_ID2	<	3.3[V]	IO Expander(PCA9539)-0 "IO1_6" pin, Pull-up	USB Board ID bit2
28	+B_VPH	>	Power:12[V]	Power connector	Power
29	+B_VPH	>	Power:12[V]	Power connector	Power
30	+B_VPH	>	Power:12[V]	Power connector	Power
58	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
59	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
60	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
27	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
57	VDD_USB_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
56	VDD_USB_CORE	>	Power:1.2[V]	1.2[V] output LDO	Power
3	GND	-	GND	GND	GND
8	GND	-	GND	GND	GND
16	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
33	GND	-	GND	GND	GND

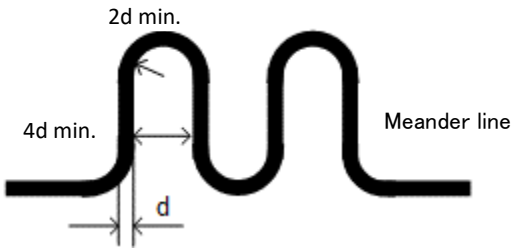
Pin	Signal Name	Direction Control - USB	Voltage	Connection of the control board	Description Example of use
42	GND	-	GND	GND	GND
45	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND

1.4. Board Layout Consideration

Due to LVDS lines on Control Board, traces on USB Board need to be designed in accordance with the following restrictions:

USB-High-Speed Differential Signal

- ・Trace Length Matching: Difference between a differential signal pair (+and -) must be 0.5[mm] maximum.
- ・Maximum Trace Length：50[mm]
- ・Differential impedance：90[Ω](90[Ω]) on Control Board side)
- ・Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically. ・Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- ・For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be twice the width of the trace. The gap between the meander traces should be at least four times the trace width.



USB-SuperSpeed Differential Signal

- ・Trace Length Matching: Difference between a differential signaling pair (+and -) must be 0.1[mm] maximum
- ・Maximum Trace Length：30[mm]・Differential Impedance：90[Ω](90[Ω] on Control Board side)
- ・Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically. ・Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- ・For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be twice the width of the trace. The gap between the meander traces should be at least four times the trace width. (as shown above)

Power Supply

- ・Comply with power supply requirements (impedance property, etc.) of the device to connect.
  If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[℃] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- ・Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.
- ・Care needs to be given for bus lines such as MII when connecting to a PCI-Express connector terminal.

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