

Revision History

Date	Revision	Comments
May 25, 2020	1.0	Initial Release

Refereneeces

No.	Document	Version	Release Date

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1. Vehicle/ Audio Board

Vehicle/Audio board is connected to Control Board, has the functions of the vehicle interface including power supply and also performing audio processing and the audio interface with external devices. These two functions can be either designed in one board or two separate boards: Vehicle Board as vehicle interface including power supply and Audio Board for audio signal processing and used as audio interface, etc.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

R-Car H3 Reference Hardware applies the one-board design for the Vehicle/Audio features.

1.1. Board Outline

The following figures show Vehicle/Audio Board dimensions. 1.2[mm] is the assumed thickness but if the design modification is required, special attention should be paid to avoid the interference with other boards.

Two 120-pin Board-to-Board connectors and one 40-pin Board-to-Board connector are used as the interfaces to Control Board and mounted on both the component side and the solder side of Vehicle/Audio Board.

The spacing between the board and chassis is shown as below (Figure 2). External interface connectors are to be placed in the position relative to the chassis.

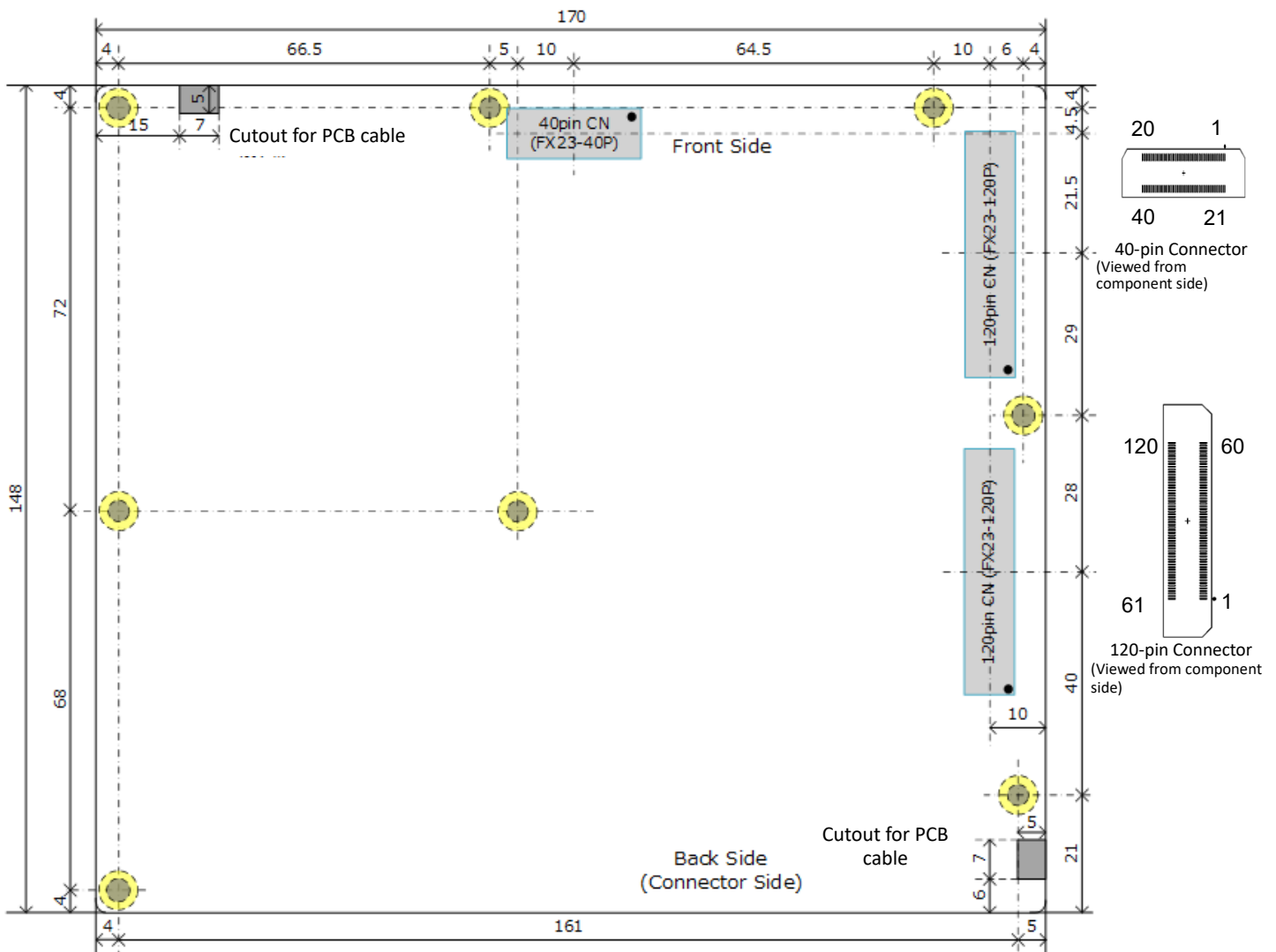


Figure 1 Vehicle/Audio Board Outline (Component side)

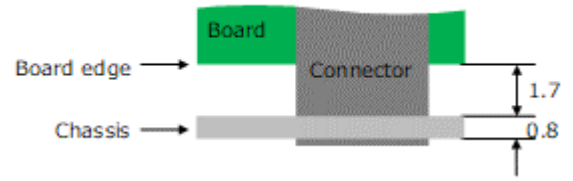
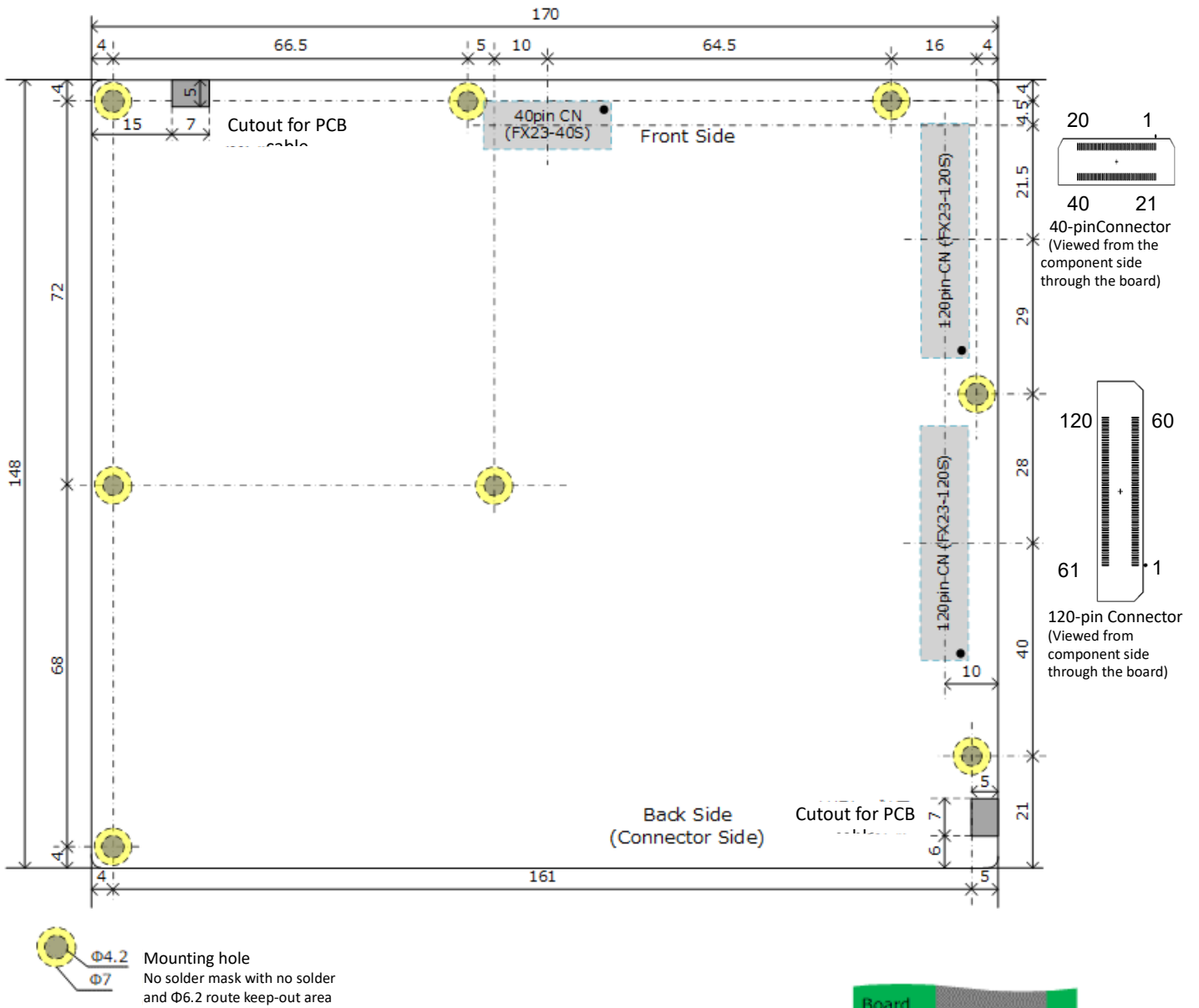


Figure 2 Vehicle/Audio Board Outline (Solder side)

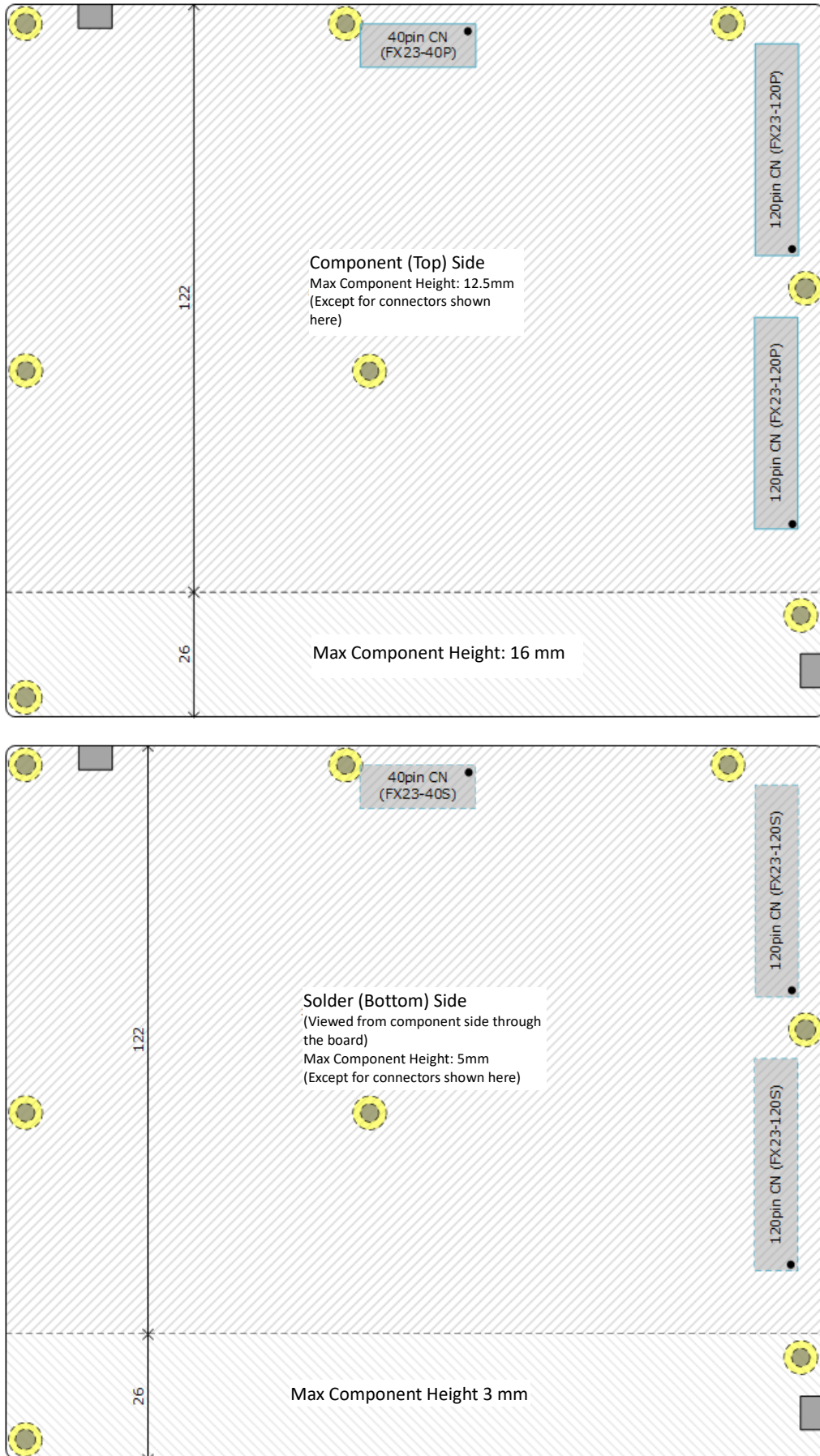


Figure 3 Vehicle/Audio Board Height Constraint

1.2. Block-to-Block Connector

Two 120-pin Board-to-Board connectors and one 40-pin Board-to-Board connector are used to connect Control Board, Vehicle Board and Audio Board. These three connectors are referred to as “block-to-block connector” in this document.

FX23 series of Hirose Electric Co., Ltd. is used for the block-to-block connector. The floating structure (± 0.6 [mm] in X and Y directions) type is used to mitigate position gap and oscillation effect.

FX23-120P-0.5SV20B and FX23-40P-0.5SV20B on component side, FX23-120S-0.5SVB and FX23-40S-0.5SVB (FX23-120S-0.5SV10B and FX23-40S-0.5SV10B are used to keep a 30mm stack height for the Control Board.) on solder side are used. A PCB with each connector should be arranged on top and bottom surface of the same axis with parallel connecting. (Same signals are assigned to all the terminals of 120pin/40pin connectors on Control board, Vehicle board, and Audio board)

Table 1 Block-to-Block Connector Specification

	FX23 Series	
	Signal	Power Supply (4 pins assigned)
Current Rating (per pin)	0.5[A]	3.0[A]
Withstand Voltage	AC150[V], 1 min	AC600[V], 1 minute
Contact Resistance	70[m Ω] or less	20[m Ω] or less
Insulation Resistance	DC100[V], 100[M Ω] or more	DC250[V], 1,000[M Ω] or more
Operating Temp:	-55 up to +105[$^{\circ}$ C]	
Floating Range	± 0.6 [mm] in X and Y directions	
Applicable Signal	8+[Gbps], Differential 100[Ω]	-

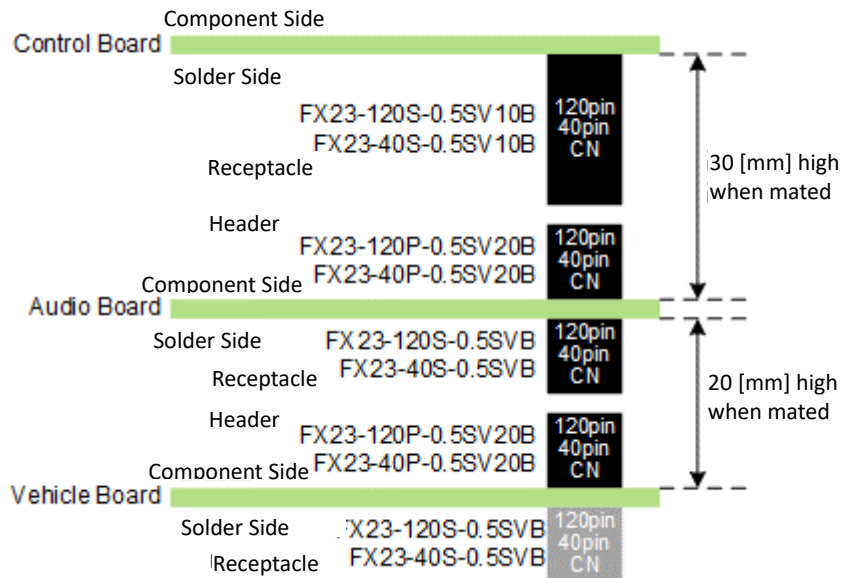


Figure 4 Block-to-Block Connector Part Number

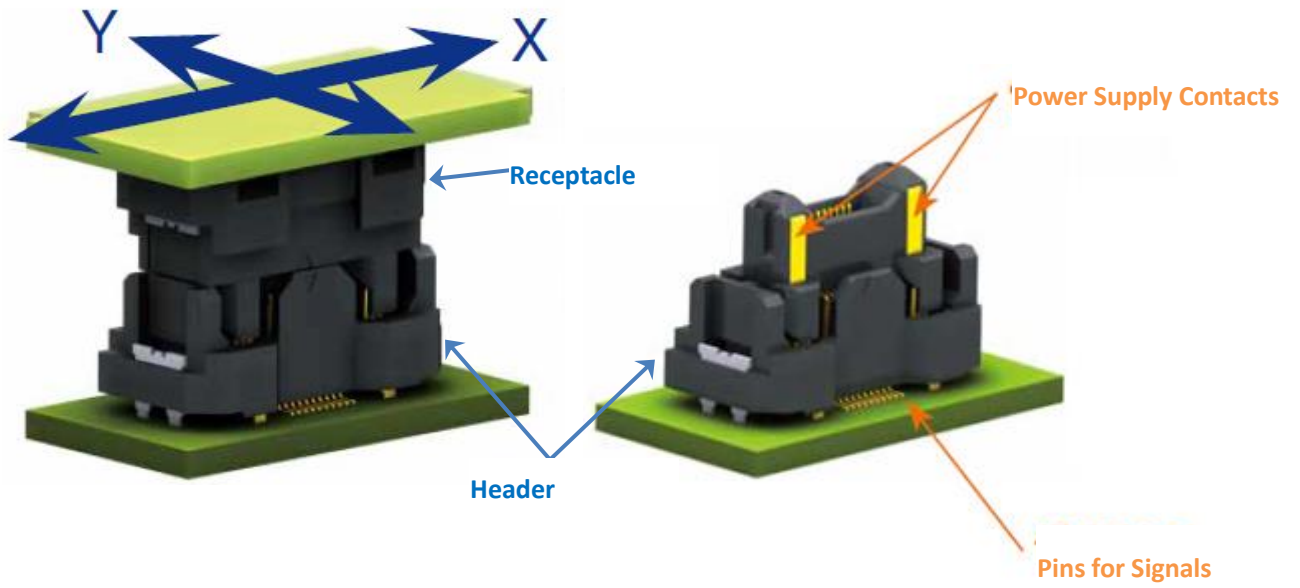


Figure 5 Block-to-Block Connector Features

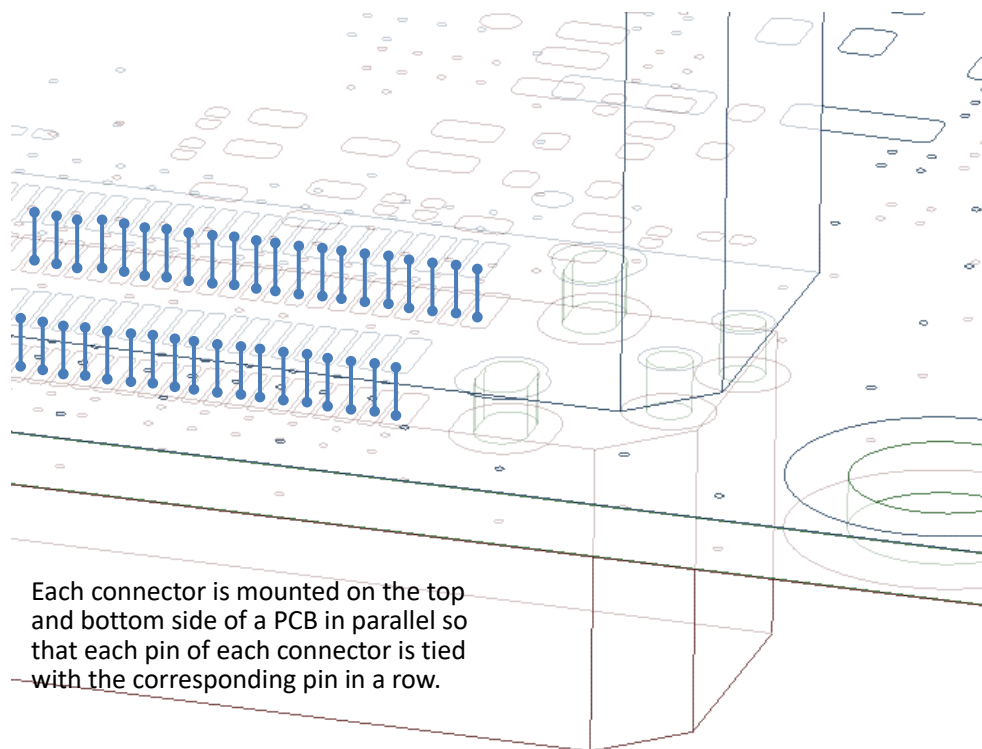
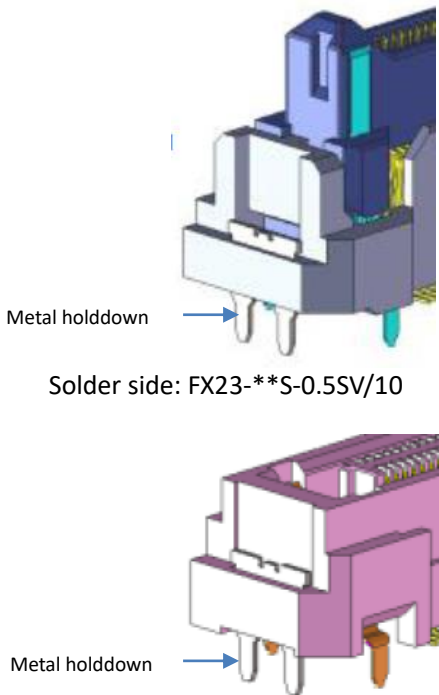


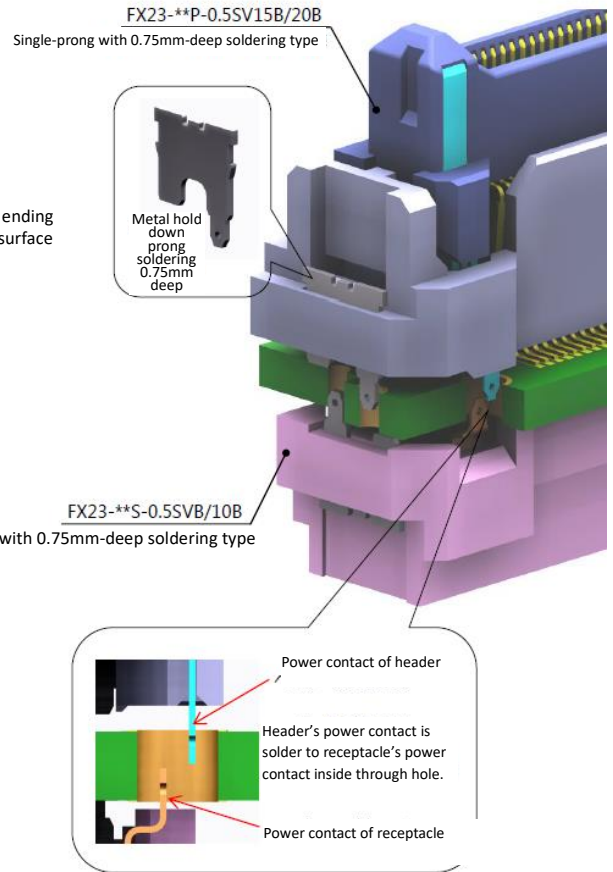
Figure 6 Block-to-Block Connector Pin Application

Component Side: FX23-**P-0.5SV20

How double-sided surface mounting works



Single-prong type (Part Number ending with the suffix "B") enables the surface mounting



The metal holddown of a standard connector has a pair of prongs which causes overlapping since the header and receptacle are mounted onto each surface of PCB in exact position of the opposite side. Thus, the suffix "B" type is used.

Figure 7 Block-to-Block Connector Consideration

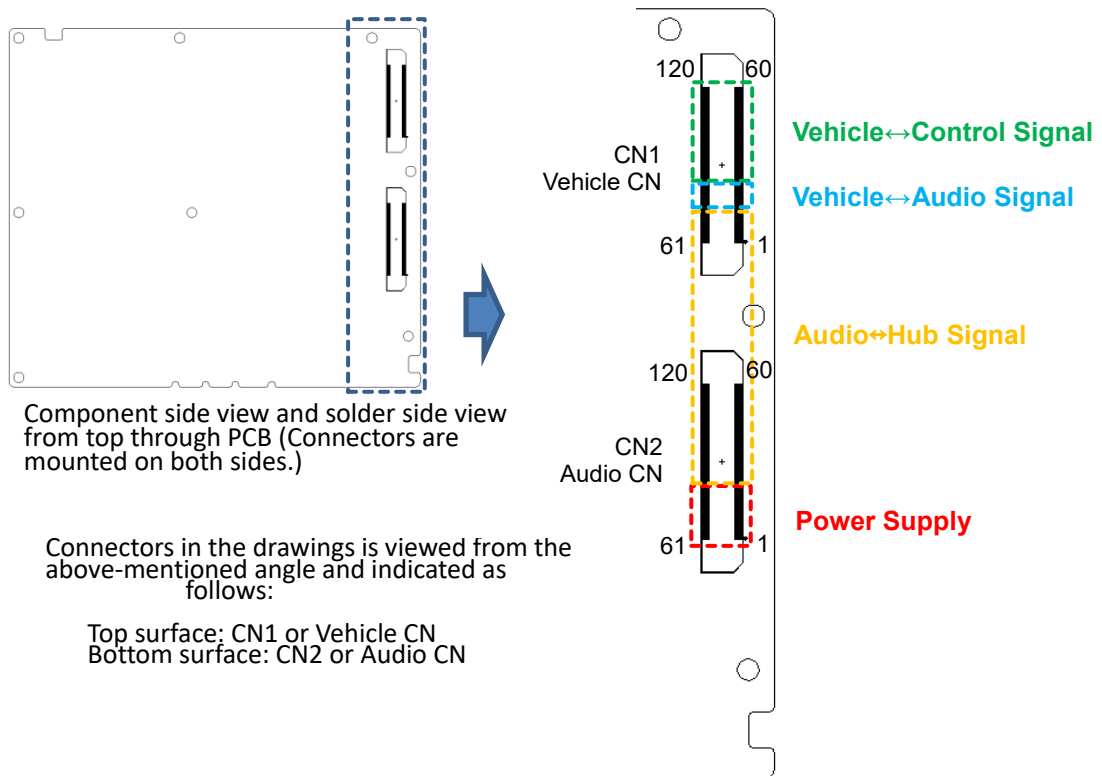


Figure 8 Block-to-Block Connector Pin Arrangement and Signal Type

1.3. Power Supply

+12[V] power supplied from a vehicle is used as a main source for Reference Hardware to run. The +12[V] from the vehicle is supplied to Vehicle Board for distributing to other boards. Components supplied +12[V] from vehicle should use withstand voltage higher than +27[V].

Power each board requires should be generated within the boards from +12[V] basically. +5.8[V] and +3.8[V] power supplies are built on Vehicle Board are connected along with +12[V] through a 120-pin connector. +5.8[V] is used for the source of commonly used +5[V] power supply and +3.8[V] is used for the source of commonly used +3.3[V] and +1.8[V] power supplies. Power IC should be designed to be non-flammable or smoke-free when shorted at output side. Use of Power IC with OCP (Over Current Protection) is recommended.

Total of 11[A] is the current capacity of the 120 pin connector can provide at +12[V] through 10 pins rated for 0.5[A/pin] and 2 pins rated for 3.0[A/pin]. If the current capacity is not enough, another dedicated connector can be added to supply +12[V].

DCDC/inductor's capacity for the source of +5V power supply line is 5.5[A], and the current capacity of 11 pins rated for 0.5[A/pin] is 5.5[A]. DCDC/inductor's capacity for the source of +3.3V power supply line is 3.5[A] and the current capacity of 7 pins rated for 0.5[A/pin] is 3.5[A]. However, as both power supplies are used in Vehicle Board (0.5[A] retained), 5.0[A] from the source of +5V power supply and 3.0[A] from the source of +3.3V power supply are the electrical current can be consumed on Audio Board and Control Board.

Power that terminals require for signaling between boards is also supplied via the 120pin connector.

Vehicle board supplies power to the terminals required for the board through the signal named as IO_VEHICLE, Audio board supplies power to its terminals through the signal named as IO_AUDIO, and Control boards supplies power to its terminals through the signals named as IO_PF (for SoC terminals), IO_VIDEO (for VideoOut board terminals) and IO_IF (USB board terminals)

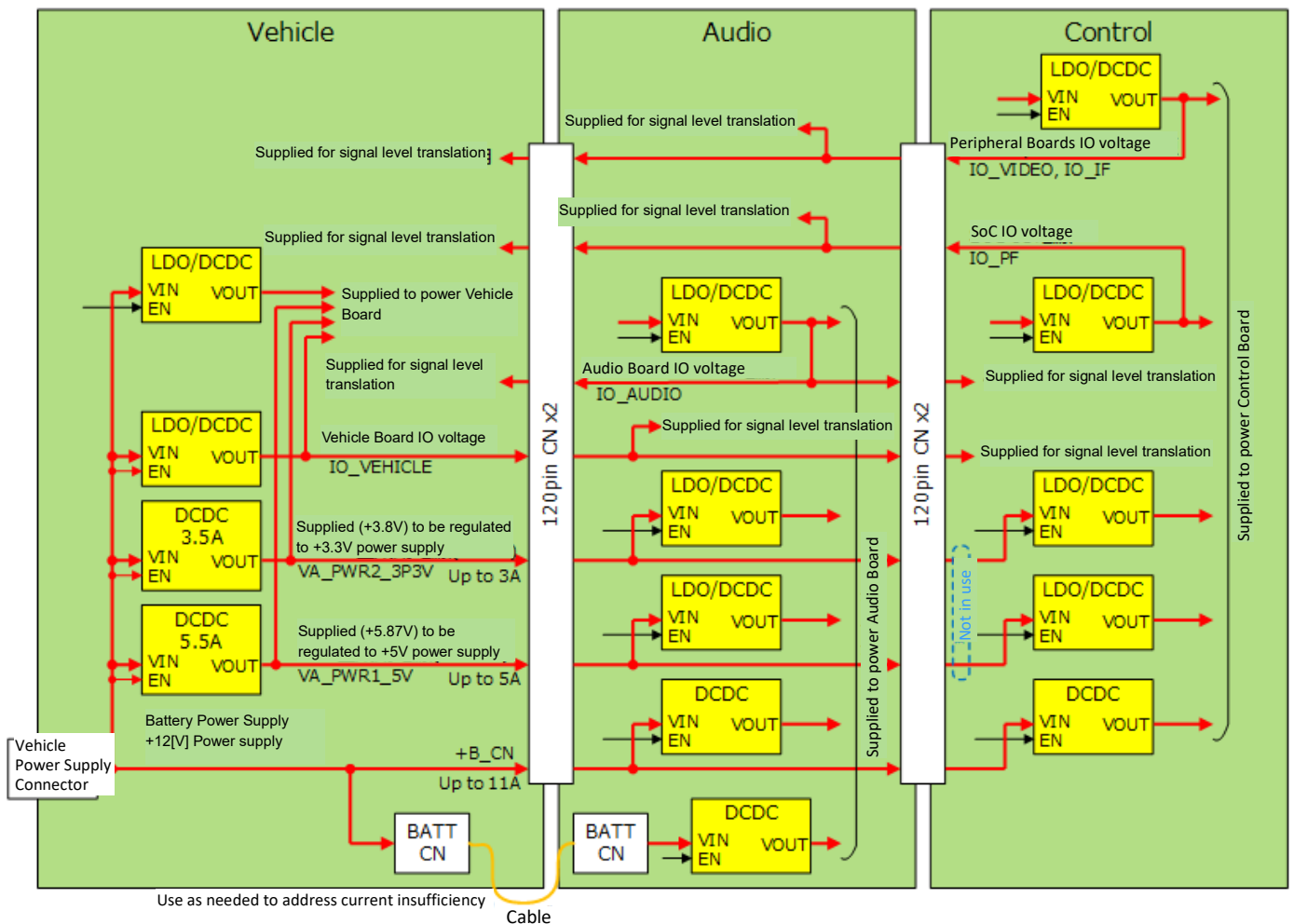


Figure 9 Power supply system

1.4. Board-to-board interface

Two 120-pin Board-to-Board connectors and one 40-pin Board-to-Board connector are connected to Control Board.

Header type connectors (Hirose Electric Co., Ltd. FX23-120P-0.5SV20B, FX23-40P-0.5SV20B) are assumed to be used on Control Board side and Receptacle connectors (Hirose Electric Co., Ltd. FX23-120S-0.5SVB, FX23-40S-0.5SVB) are assumed to be used on the other side..

This connector enables 8[Gbps] physical transmission. The floating structure allows the connector to be adjusted up to ± 0.6 [mm] in the X and Y directions so as to mitigate the gap. Current rating of a signal pin is 500[mA], and 3.0 [A] for a power supply pin.

WLAN Board and GNSS Board are connected to external antenna via Vehicle Board. Thus, a connector to connect WLAN Board and WLAN Board with a coaxial cable and an external antenna connector should be mounted on Vehicle Board. I-PEX 20279-001E is to be used for the coaxial cable connector.

Reference Hardware Design Guideline for Vehicle/Audio Board

1.4.1. Vehicle/Audio board interface (R-Car H3 Reference Hardware)

The schematic of Vehicle/Audio Board on R-Car H3 Reference Hardware Control Board side is shown in Figure 10, Figure 12 and Figure 13, and the pin assignments and the connected terminals are listed on Table 2.

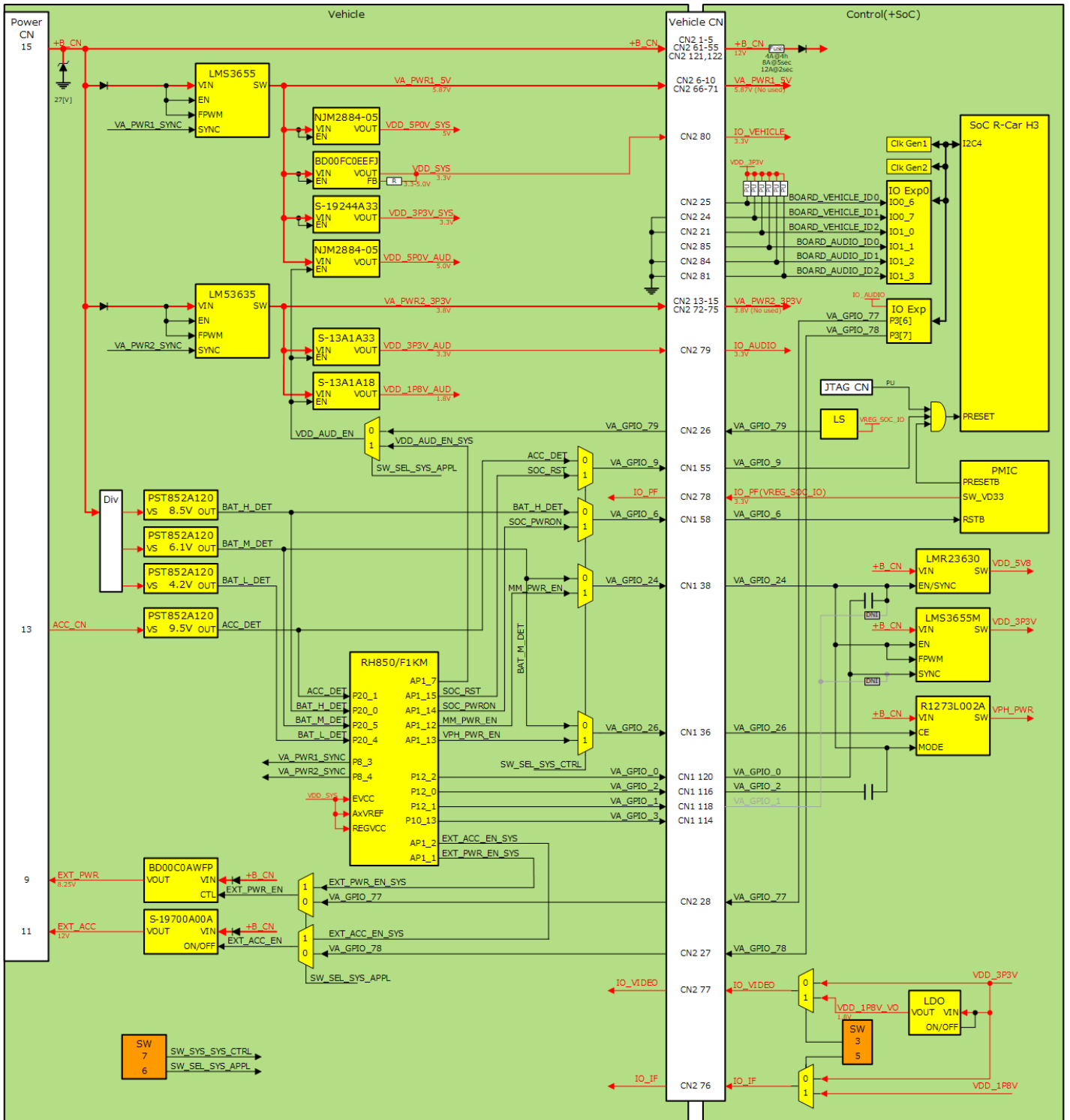


Figure 10 Connectivity between Vehicle/Audio Board and Control Board (for power supplies on R-Car H3 Reference Hardware)

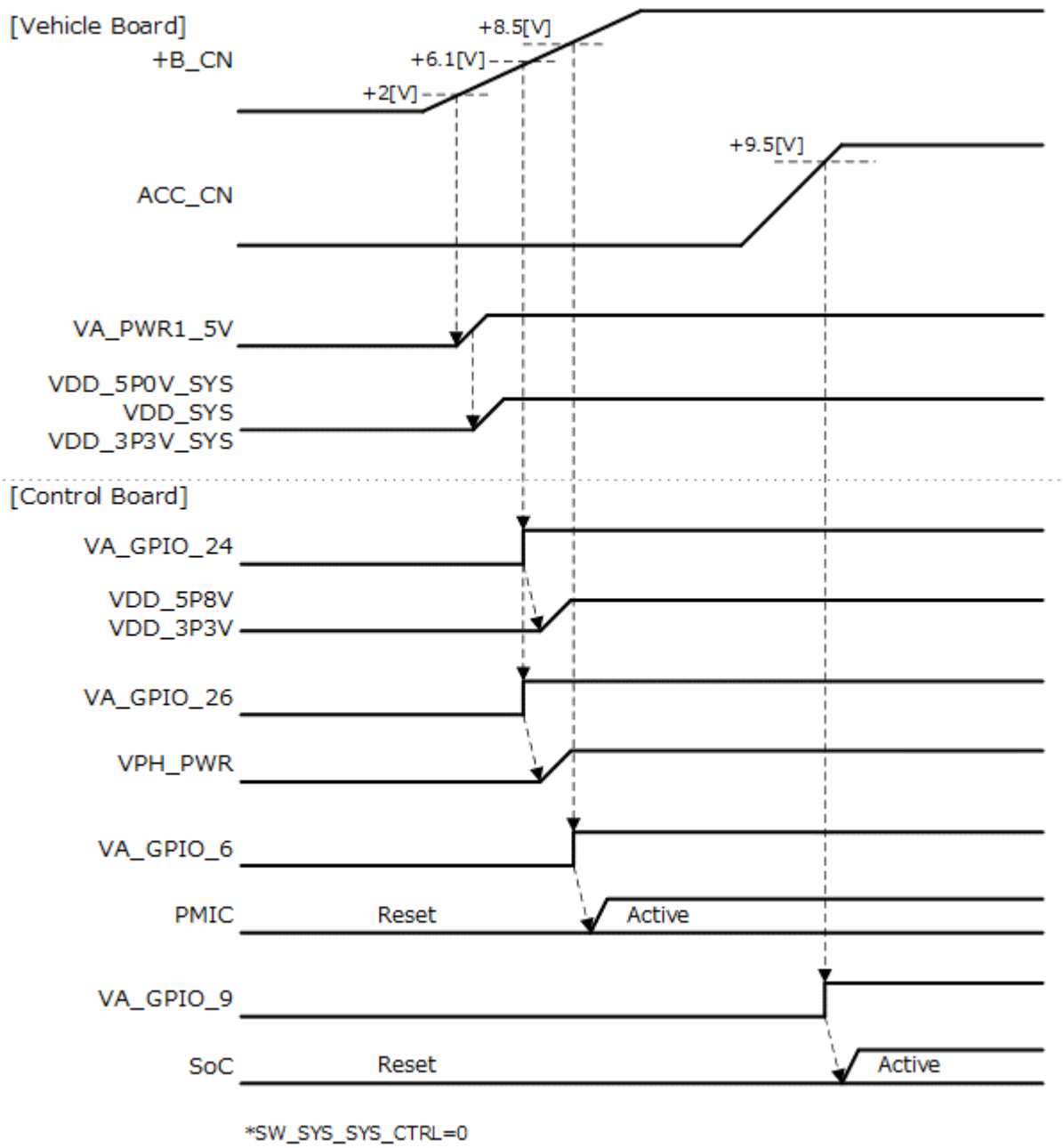


Figure 11 Power ON Sequence (R-Car H3 Reference Hardware)

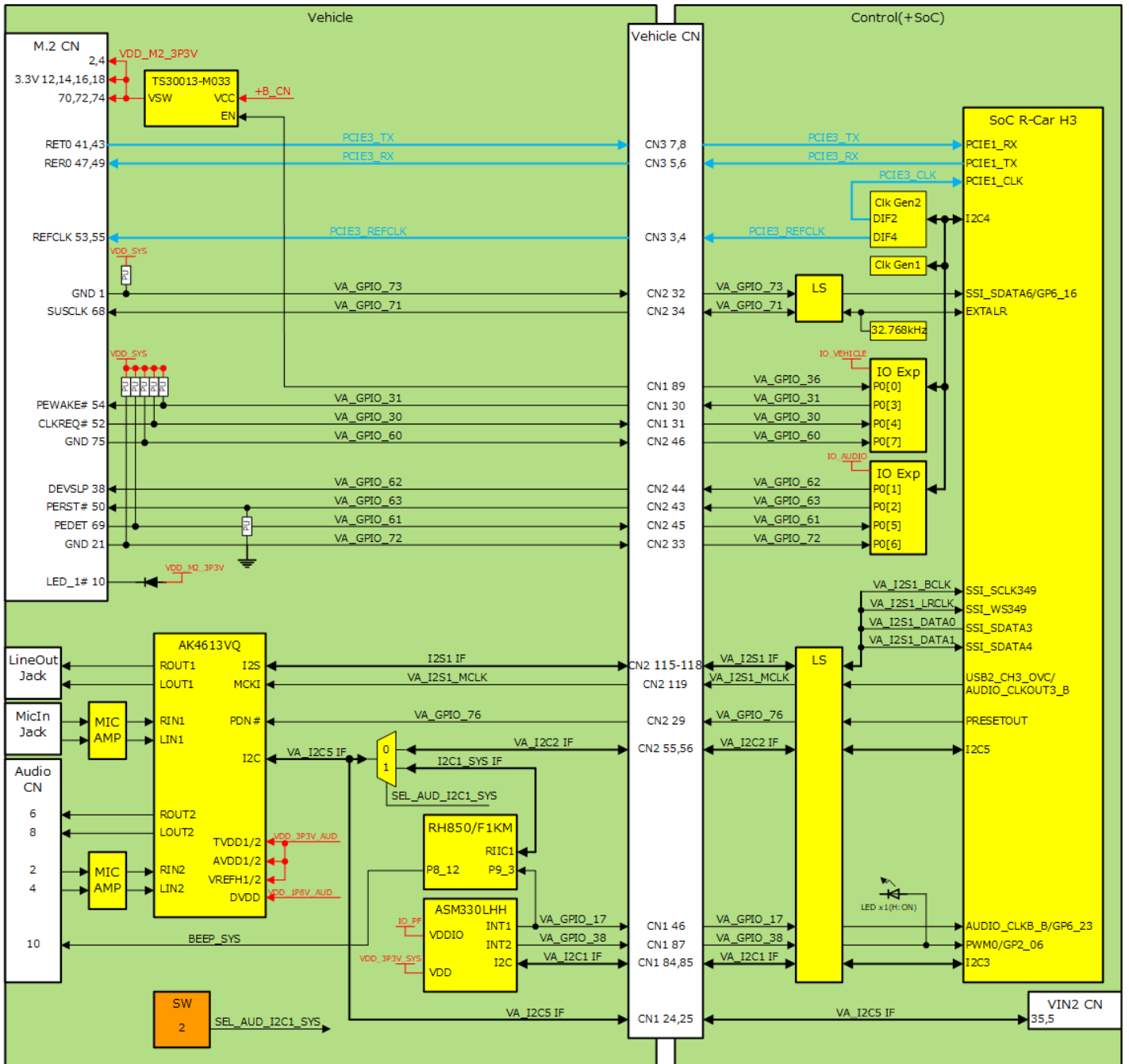


Figure 13 Connectivity between Vehicle/Audio Board and Control Board (for Audios on R-Car H3 Reference Hardware)

Reference Hardware Design Guideline for Vehicle/Audio Board

Table 2 Connector (Vehicle/ Audio CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware))

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
1	1	VA_UART6_RX	3.3[V]	RS485(2) transceiver(ST3485EI) receiver output pin, Pull-down	>	R-Car H3 "USB0_OVC/HRX2_C" pin, Pull-down
1	2	VA_UART5_RX	3.3[V]	NC	-	No used
1	3	VA_UART5_TX	3.3[V]	NC	-	No used
1	4	VA_UART4_RX	3.3[V]	RS485(1) transceiver(ST3485EI) receiver output pin, Pull-down	>	R-Car H3 "MSIOF0_SS1/RX5_A" pin
1	5	VA_UART4_TX	3.3[V]	RS485(1) transceiver(ST3485EI) driver input pin, Pull-down	<	R-Car H3 "MSIOF0_SS2/TX5_A" pin
1	6	GND	-	GND	-	GND
1	7	VA_SPI4_VAI	3.3[V]	RH850 "P0_1/CSIH0SI"pin	↔	No used
1	8	VA_SPI4_VAO	3.3[V]	RH850 "P0_3/CSIH0SO"pin	↔	No used
1	9	VA_SPI4_CS	3.3[V]	RH850 "P8_2/CSIH0CSS0"pin	↔	No used
1	10	VA_SPI4_CLK	3.3[V]	RH850 "P0_2/CSIH0SC"pin	↔	No used
1	11	GND	-	GND	-	GND
1	12	GND	-	GND	-	GND
1	13	VA_GPIO_59	3.3[V]	RH850 "P0_4"pin	↔	NC
1	14	VA_GPIO_58	3.3[V]	RH850 "P12_3"pin	↔	NC
1	15	VA_GPIO_57	3.3[V]	RH850 "P11_9"pin	↔	NC
1	16	VA_GPIO_56	3.3[V]	RH850 "P11_8"pin	↔	NC
1	17	VA_GPIO_55	3.3[V]	RH850 "P11_0"pin	↔	NC
1	18	VA_GPIO_54	3.3[V]	RH850 "P10_15"pin	↔	NC
1	19	VA_GPIO_53	3.3[V]	RH850 "P18_6"pin	↔	NC
1	20	VA_GPIO_52	3.3[V]	RH850 "AP1_0"pin	↔	NC
1	21	VA_GPIO_51	3.3[V]	RH850 "AP1_5"pin	↔	NC
1	22	VA_GPIO_50	3.3[V]	RH850 "AP1_6"pin	↔	NC
1	23	GND	-	GND	-	GND
1	24	VA_I2C5_SDA	3.3[V]	No used	-	No used
1	25	VA_I2C5_SCL	3.3[V]	No used	-	No used
1	26	GPANA_06	-	NC	-	NC
1	27	GPANA_05	-	NC	-	NC

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
1	28	GPANA_04	-	NC	-	NC
1	29	GPANA_03	-	NC	-	NC
1	30	VA_GPIO_31	3.3[V]	M.2 CN 54pin(PEWAKE#), Pull-up	<	IO Expander-0 bit3
1	31	VA_GPIO_30	3.3[V]	M.2 CN 52pin(CLKREQ#), Pull-up	>	IO Expander-0 bit2
1	32	VA_GPIO_29	3.3[V]	RH850 "P10_8/FLMD1"pin, Pull-down	<>	IO Expander-0 bit1
1	33	VA_GPIO_28	3.3[V]	RH850 "P10_6"pin	<>	IO Expander-0 bit0
1	34	GND	-	GND	-	GND
1	35	VA_GPIO_27	3.3[V]	RH850 "P20_2"pin	<>	Control of USB-Debug mode
1	36	VA_GPIO_26	3.3[V]	+B voltage detect(6.1V), RH850 "P20_5"pin	>	DCDC(VPH_PWR) enable pin
1	37	VA_GPIO_25	3.3[V]	RH850 "P20_3"pin	<>	Voltage detect(VDD_3P3V) "OUT" pin
1	38	VA_GPIO_24	3.3[V]	+B voltage detect(6.1V), RH850 "P20_5"pin	>	DCDC(VDD_5P8V,VDD_3P3V) enable pin
1	39	VA_GPIO_23	3.3[V]	NC	-	IO Expander-2 bit6
1	40	VA_GPIO_22	3.3[V]	NC	-	IO Expander-2 bit5
1	41	VA_GPIO_21	3.3[V]	NC	-	IO Expander-2 bit4
1	42	VA_GPIO_20	3.3[V]	NC	-	IO Expander-2 bit3
1	43	GND	-	GND	-	GND
1	44	VA_GPIO_19	3.3[V]	NC	-	IO Expander-2 bit2
1	45	VA_GPIO_18	3.3[V]	NC	-	IO Expander-2 bit1
1	46	VA_GPIO_17	3.3[V]	6-axis sensor(ASM330L) "INT1"pin, RH850 ""pin	>	R-Car H3 "AUDIO_CLK_B/GP6_23" pin
1	47	VA_GPIO_16	3.3[V]	RH850 "P8_7"pin	<>	IO Expander-2 bit0
1	48	VA_GPIO_15	3.3[V]	NC	-	IO Expander-1 bit7
1	49	VA_GPIO_14	3.3[V]	RH850 "P8_6"pin	<>	R-Car H3 "NMI" pin
1	50	VA_GPIO_13	3.3[V]	RH850 "JP0_6"pin	<>	IO Expander-1 bit6
1	51	VA_GPIO_12	3.3[V]	RH850 "P2_2"pin	<>	IO Expander-1 bit5
1	52	VA_GPIO_11	3.3[V]	RH850 "P2_3"pin	<>	IO Expander-1 bit4
1	53	GND	-	GND	-	GND
1	54	VA_GPIO_10	3.3[V]	RH850 "P1_8"pin	<>	IO Expander-1 bit3

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
1	55	VA_GPIO_9	3.3[V]	ACC voltage detect(9.5V), RH850 "P20_1"pin	>	R-Car H3 "PRESET#" pin, Pull-up
1	56	VA_GPIO_8	3.3[V]	RH850 "P2_1"pin	<>	IO Expander-1 bit2
1	57	VA_GPIO_7	3.3[V]	RH850 "JP0_4"pin	<>	IO Expander-1 bit1
1	58	VA_GPIO_6	3.3[V]	+B voltage detect(8.5V), RH850 "P20_0"pin	>	PMIC "RSTB" pin
1	59	VA_GPIO_5	3.3[V]	RH850 "P8_11"pin	<>	IO Expander-1 bit0
1	60	VA_GPIO_4	3.3[V]	RH850 "P1_2"pin	<>	R-Car H3 "SSI_SDATA2_A/GP6_04" pin
1	61	VA_UART6_TX	3.3[V]	RS485(2) transceiver(ST3485EI) driver input pin, Pull-down	<	R-Car H3 "USB1_PWEN(HTX2_C" pin
1	62	VA_SPI3_VAI	3.3[V]	NC	-	No used
1	63	VA_SPI3_VAO	3.3[V]	NC	-	No used
1	64	VA_SPI3_CS	3.3[V]	NC	-	No used
1	65	VA_SPI3_CLK	3.3[V]	NC	-	No used
1	66	GND	-	GND	-	GND
1	67	VA_SPI2_VAI	3.3[V]	NC	-	No used
1	68	VA_SPI2_VAO	3.3[V]	NC	-	No used
1	69	VA_SPI2_CS	3.3[V]	NC	-	No used
1	70	VA_SPI2_CLK	3.3[V]	NC	-	No used
1	71	GND	-	GND	-	GND
1	72	GND	-	GND	-	GND
1	73	VA_GPIO_49	3.3[V]	RH850 "P0_6"pin	<>	NC
1	74	VA_GPIO_48	3.3[V]	RH850 "P0_5"pin	<>	NC
1	75	VA_GPIO_47	-	NC	-	NC
1	76	VA_GPIO_46	-	NC	-	NC
1	77	VA_GPIO_45	3.3[V]	RH850 "AP1_7"pin	<>	NC
1	78	VA_GPIO_44	3.3[V]	RH850 "AP1_8"pin	<>	NC
1	79	VA_GPIO_43	-	NC	-	NC
1	80	VA_GPIO_42	-	NC	-	NC
1	81	VA_GPIO_41	-	NC	-	NC
1	82	VA_GPIO_40	-	NC	-	NC

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
1	83	GND	-	GND	-	GND
1	84	VA_I2C1_SDA	3.3[V]	6-axis sensor(ASM330L) "SDA"pin	<>	R-Car H3 "PWM2_A/SDA3" pin, Pull-up
1	85	VA_I2C1_SCL	3.3[V]	6-axis sensor(ASM330L) "SCL"pin	<>	R-Car H3 "PWM1_A/SCL3" pin, Pull-up
1	86	VA_GPIO_39	3.3[V]	NC	-	IO Expander-2 bit7
1	87	VA_GPIO_38	3.3[V]	6-axis sensor(ASM330L) "INT2"pin	>	R-Car H3 "PWM0/GP2_06" pin
1	88	VA_GPIO_37	3.3[V]	LIN transceiver(TJA1029T) "SLP_N"pin, Pull-down	<	R-Car H3 "SSI_SCK6/GP6_14" pin
1	89	VA_GPIO_36	3.3[V]	DCDC for M.2 "EN"pin	<	IO Expander-0 bit4
1	90	VA_I2C4_SDA	3.3[V]	Vehicle CN2 9pin, Pull-up	<>	R-Car H3 "MLB_SIG/SDA1_B" pin, Pull-up
1	91	VA_I2C4_SCL	3.3[V]	Vehicle CN2 7pin, Pull-up	<>	R-Car H3 "MLB_CLK/SCL1_B" pin, Pull-up
1	92	VA_UART10_RX	3.3[V]	LIN transceiver(TJA1029T) receive data output pin, Pull-up	>	R-Car H3 "MLB_SIG/RX1_B" pin, Pull-up
1	93	VA_UART10_TX	3.3[V]	LIN transceiver(TJA1029T) transmit data input pin	<	R-Car H3 "MLB_DAT/TX1_B" pin
1	94	GND	-	GND	-	GND
1	95	VA_UART9_RX	3.3[V]	RH850 "P10_12/RLIN31TX"pin	>	No used
1	96	VA_UART9_TX	3.3[V]	RH850 "P10_11/RLIN31RX"pin	<	No used
1	97	VA_UART3_RX	3.3[V]	CAN(1) transceiver(TCAN1042) receive data output pin	>	R-Car H3 "RD_WR#/CANFD0_RX_A" pin
1	98	VA_UART3_TX	3.3[V]	CAN(1) transceiver(TCAN1042) receive data output pin	<	R-Car H3 "RD#/CANFD0_TX_A" pin
1	99	VA_UART2_RX	3.3[V]	CAN(2) transceiver(TCAN1042) receive data output pin	>	R-Car H3 "WE1#/CANFD1_RX" pin
1	100	VA_UART2_TX	3.3[V]	CAN(2) transceiver(TCAN1042) receive data output pin	<	R-Car H3 "BS#/CANFD1_TX" pin
1	101	VA_UART1_RX	3.3[V]	RH850 "P10_10/RLIN30TX"pin	>	R-Car H3 "USB0_OVC/HRX2_C" pin
1	102	VA_UART1_TX	3.3[V]	RH850 "P10_9/RLIN30RX"pin	<	R-Car H3 "USB1_PWEN/HTX2_C" pin
1	103	GND	-	GND	-	GND
1	104	VA_SPI5_VAI	3.3[V]	RH850 "P11_4/CSIH2SI"pin	<	R-Car H3 "D3/MSIOF3_TXD_A" pin
1	105	VA_SPI5_VAO	3.3[V]	RH850 "P11_2/CSIH2SO"pin	>	R-Car H3 "D2/MSIOF3_RXD_A" pin
1	106	VA_SPI5_CS	3.3[V]	RH850 "P9_2/CSIH2CSS2"pin	<>	R-Car H3 "D1/MSIOF3_SYNC_A" pin

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
1	107	VA_SPI5_CLK	3.3[V]	RH850 "P11_3/CSIH2SC"pin	<>	R-Car H3 "D0/MSIOF3_SCK_A" pin
1	108	GND	-	GND	-	GND
1	109	VA_SPI1_VAI	3.3[V]	RH850 "P11_5/CSIH3SI"pin	<	R-Car H3 "RTS1#/MSIOF1_TXD_B" pin
1	110	VA_SPI1_VAO	3.3[V]	RH850 "P11_6/CSIH3SO"pin	>	R-Car H3 "CTS1#/MSIOF1_RXD_B" pin
1	111	VA_SPI1_CS	3.3[V]	RH850 "P10_14/CSIH3SSI"pin	<>	R-Car H3 "CTS0#/MSIOF1_SYNC_B" pin
1	112	VA_SPI1_CLK	3.3[V]	RH850 "P11_7/CSIH3SC"pin	<>	R-Car H3 "SCK2/MSIOF1_SCK_B" pin
1	113	GND	-	GND	-	GND
1	114	VA_GPIO_3	3.3[V]	RH850 "P10_13"pin	>	NC
1	115	GND	-	GND	-	GND
1	116	VA_GPIO_2	3.3[V]	RH850 "P12_0"pin	>	DCDC(R1273L(VPH_PWR)) "MODE" pin (sync clock)
1	117	GND	-	GND	-	GND
1	118	VA_GPIO_1	3.3[V]	RH850 "P12_1"pin	>	No used
1	119	GND	-	GND	-	GND
1	120	VA_GPIO_0	3.3[V]	RH850 "P12_2"pin	>	DCDC(LMS3655(VDD_3P3V)) "SYNC" pin, DCDC(LMR23630(VDD_5P8V)) "EN/SYNC" pin
1	121	GND	-	GND	-(Power pin)	GND
1	122	GND	-	GND	-(Power pin)	GND
1	123	GND	-	GND	-(Power pin)	GND
1	124	GND	-	GND	-(Power pin)	GND
2	1	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	2	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	3	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	4	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	5	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	6	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	7	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	8	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	9	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	10	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	11	Reserved	-	NC	-	NC
2	12	Reserved	-	NC	-	NC
2	13	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	14	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	15	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	16	Reserved	-	NC	-	NC
2	17	Reserved	-	NC	-	NC
2	18	Reserved	-	NC	-	NC
2	19	USB4_D_M	-	NC	-	NC
2	20	USB4_D_P	-	NC	-	NC
2	21	BOARD_VEHICLE_ID2	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO1_0" pin, Pull-up
2	22	GND	-	GND	-	GND
2	23	GND	-	GND	-	GND
2	24	BOARD_VEHICLE_ID1	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO0_7" pin, Pull-up
2	25	BOARD_VEHICLE_ID0	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO0_6" pin, Pull-up
2	26	VA_GPIO_79	3.3[V]	5.0V/3.3V/1.8V LDO for Audio enable(H:Enable)	<	Fixed H
2	27	VA_GPIO_78	3.3[V]	LDO for EXT_ACC enable(H:Enable)	<	IO Expander-3 bit7
2	28	VA_GPIO_77	3.3[V]	LDO for EXT_PWR enable(H:Enable)	<	IO Expander-3 bit6

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	29	VA_GPIO_76	3.3[V]	Audio codec(AK4613VQ) "PDN#"pin, Pull-down	<	R-Car H3 "PRESETOUT#" pin
2	30	VA_GPIO_75	3.3[V]	RS485(2) transceiver(ST3485EI) driver output enable pin, Pull-down	<	R-Car H3 "SSI_SDAT5/GP6_13" pin
2	31	VA_GPIO_74	3.3[V]	RS485(2) transceiver(ST3485EI) receiver output enable pin, Pull-up	<	R-Car H3 "SSI_SCK5/GP6_11" pin
2	32	VA_GPIO_73	3.3[V]	M.2 CN 1pin(GND), Pull-up	>	R-Car H3 "SSI_SDAT6/GP6_16" pin
2	33	VA_GPIO_72	3.3[V]	M.2 CN 21pin(GND), Pull-up	>	IO Expander-3 bit5
2	34	VA_GPIO_71	3.3[V]	M.2 CN 68pin(SUSCLK)	<	32.768kHz X'tal
2	35	GND	-	GND	-	GND
2	36	VA_GPIO_70	3.3[V]	NC	-	IO Expander-3 bit4
2	37	VA_GPIO_69	3.3[V]	No used	-	IO Expander-3 bit3
2	38	VA_GPIO_68	3.3[V]	CAN(1) transceiver(TCAN1042) standby mode pin(H:Standby), Pull-up	<	R-Car H3 "SSI_SDAT9_A/GP6_21" pin
2	39	VA_GPIO_67	3.3[V]	CAN(2) transceiver(TCAN1042) standby mode pin(H:Standby), Pull-up	<	R-Car H3 "SSI_WS5/GP6_12" pin
2	40	VA_GPIO_66	3.3[V]	IEBus transceiver(CA0013BM) standby pin(L:Standby), Pull-up	<	IO Expander-3 bit2
2	41	VA_GPIO_65	3.3[V]	RS485(1) transceiver(ST3485EI) driver output enable pin, Pull-down	<	R-Car H3 "MSIOF0_TXD/GP5_20" pin
2	42	VA_GPIO_64	3.3[V]	RS485(1) transceiver(ST3485EI) receiver output enable pin, Pull-up	<	R-Car H3 "MSIOF0_RXD/GP5_22" pin
2	43	VA_GPIO_63	3.3[V]	M.2 CN 50pin(PERST#), Pull-down	<	IO Expander-0 bit7
2	44	VA_GPIO_62	3.3[V]	M.2 CN 38pin(DEVSLP)	<	IO Expander-3 bit1
2	45	VA_GPIO_61	3.3[V]	M.2 CN 69pin(PEDET), Pull-up	>	IO Expander-0 bit6
2	46	VA_GPIO_60	3.3[V]	M.2 CN 75pin(GND), Pull-up	>	IO Expander-0 bit5
2	47	GND	-	GND	-	GND
2	48	VA_I2S3_DATA1	3.3[V]	NC	-	No used
2	49	VA_I2S3_DATA0	3.3[V]	NC	-	No used

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	50	VA_I2S3_LRCLK	3.3[V]	NC	-	No used
2	51	VA_I2S3_BCLK	3.3[V]	NC	-	No used
2	52	GND	-	GND	-	GND
2	53	VA_I2C3_SDA	3.3[V]	RH850 "P0_11/RIICOSDA"pin, Pull-up	<>	No used
2	54	VA_I2C3_SCL	3.3[V]	RH850 "P0_12/RIICOSCL"pin, Pull-up	<>	No used
2	55	VA_I2C2_SDA	3.3[V]	Audio codec(AK4613VQ) "SDA/CDTI"pin, Pull-up	<>	R-Car H3 "AVB_AVTP_CAPTURE_A/SDA5" pin, Pull-up
2	56	VA_I2C2_SCL	3.3[V]	Audio codec(AK4613VQ) "SCL/CCLK"pin, Pull-up	<>	R-Car H3 "AVB_AVTP_MATCH_A/SCL5" pin, Pull-up
2	57	VA_UART8_RX	3.3[V]	IEBus transceiver(CA0013BM) data output pin, Pull-up	>	No used
2	58	VA_UART8_TX	3.3[V]	IEBus transceiver(CA0013BM) data input pin	<	No used
2	59	VA_UART7_RX	3.3[V]	NC	-	No used
2	60	VA_UART7_TX	3.3[V]	NC	-	No used
2	61	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	62	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	63	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	64	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	65	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>	DCDCs/LDOs VIN
2	66	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	67	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	68	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	69	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	70	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	71	VA_PWR1_5V	5.87[V]	DCDC(LMS3655(VA_PWR1_5V)) VOUT	>	No used
2	72	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	73	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	74	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	75	VA_PWR2_3P3V	3.8V	DCDC(LM53635(VA_PWR2_3P3V)) VOUT	>	No used
2	76	IO_IF	3.3[V]	NC	<	LDO VOUT(VDD_USB_IOBANK)
2	77	IO_VIDEO	3.3[V]	NC	<	LDO VOUT(VDD_VOUT_IOBANK)
2	78	IO_PF	3.3[V]	Level shifter VCC	<	PMIC VOUT(VREG_SOC_IO)
2	79	IO_AUDIO	3.3[V]	LDO VOUT	>	Level shifter VCC
2	80	IO_VEHICLE	3.3[V]	LDO VOUT	>	Level shifter VCC
2	81	BOARD_AUDIO_ID2	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO1_3" pin, Pull-up
2	82	GND	-	GND	-	GND
2	83	GND	-	GND	-	GND
2	84	BOARD_AUDIO_ID1	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO1_2" pin, Pull-up
2	85	BOARD_AUDIO_ID0	3.3[V]	GND	>	IO Expander(PC9539)-0 "IO1_1" pin, Pull-up
2	86	VA_I2S7_DATA	-	NC	-	NC
2	87	VA_I2S7_LRCLK	-	NC	-	NC
2	88	VA_I2S7_BCLK	-	NC	-	NC
2	89	GND	-	GND	-	GND
2	90	VA_I2S6_DATA	-	NC	-	NC
2	91	VA_I2S6_LRCLK	-	NC	-	NC
2	92	VA_I2S6_BCLK	-	NC	-	NC

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	93	GND	-	GND	-	GND
2	94	VA_I2S5_DATA	-	NC	-	NC
2	95	VA_I2S5_LRCLK	-	NC	-	NC
2	96	VA_I2S5_BCLK	-	NC	-	NC
2	97	GND	-	GND	-	GND
2	98	VA_I2S4_DATA	3.3[V]	NC	-	No used
2	99	VA_I2S4_LRCLK	3.3[V]	NC	-	No used
2	100	VA_I2S4_BCLK	3.3[V]	NC	-	No used
2	101	GND	-	GND	-	GND
2	102	VA_I2S8_DATA1	3.3[V]	NC	-	No used
2	103	VA_I2S8_DATA0	3.3[V]	NC	-	No used
2	104	VA_I2S8_LRCLK	3.3[V]	NC	-	No used
2	105	VA_I2S8_BCLK	3.3[V]	NC	-	No used
2	106	VA_I2S8_MCLK	3.3[V]	NC	-	No used
2	107	GND	-	GND	-	GND
2	108	VA_I2S2_DATA1	3.3[V]	NC	-	No used
2	109	VA_I2S2_DATA0	3.3[V]	NC	-	No used
2	110	VA_I2S2_LRCLK	3.3[V]	NC	-	No used
2	111	VA_I2S2_BCLK	3.3[V]	NC	-	No used
2	112	GND	-	GND	-	GND
2	113	VA_I2S1_DATA3	3.3[V]	Audio codec(AK4613VQ) "SDTO2"pin	>	No used
2	114	VA_I2S1_DATA2	3.3[V]	Audio codec(AK4613VQ) "SDTI2"pin	<	No used
2	115	VA_I2S1_DATA1	3.3[V]	Audio codec(AK4613VQ) "SDTO1"pin	>	R-Car H3 "SSI_SDATA4" pin
2	116	VA_I2S1_DATA0	3.3[V]	Audio codec(AK4613VQ) "SDTI1"pin	<	R-Car H3 "SSI_SDATA3" pin
2	117	VA_I2S1_LRCLK	3.3[V]	Audio codec(AK4613VQ) "LRCK"pin	<>	R-Car H3 "SSI_WS34" pin
2	118	VA_I2S1_BCLK	3.3[V]	Audio codec(AK4613VQ) "BICK"pin	<>	R-Car H3 "SSI_SCK349" pin
2	119	VA_I2S1_MCLK	3.3[V]	Audio codec(AK4613VQ) "MCKI/XTI"pin	<	R-Car H3 "USB2_CH3_OVC/AUDIO_CLKOUT3_B" pin
2	120	Reserved	-	NC	-	NC
2	121	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>(Power pin)	DCDCs/LDOs VIN

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
2	122	GND	-	GND	-(Power pin)	GND
2	123	+B_CN	12[V]	Power input from vehicle, DCDCs/LDOs VIN	>(Power pin)	DCDCs/LDOs VIN
2	124	GND	-	GND	-(Power pin)	GND
3	1	SHDN	-	NC	-	NC
3	2	GND	-	GND	-	GND
3	3	PCIE3_REFCLK_P	LVDS	M.2 CN 55pin(REFCLKp)	<	Clock-generator2 "DIF4+" pin
3	4	PCIE3_REFCLK_M	LVDS	M.2 CN 53pin(REFCLKn)	<	Clock-generator2 "DIF4-" pin
3	5	PCIE3_RX0_P	LVDS	M.2 CN 49pin(PERp0)	<	R-Car H3 "PCIE1_TX_P" pin
3	6	PCIE3_RX0_M	LVDS	M.2 CN 47pin(PERn0)	<	R-Car H3 "PCIE1_TX_M" pin
3	7	PCIE3_TX0_P	LVDS	M.2 CN 43pin(PETp0)	>	R-Car H3 "PCIE1_RX_P" pin
3	8	PCIE3_TX0_M	LVDS	M.2 CN 41pin(PETn0)	>	R-Car H3 "PCIE1_RX_M" pin
3	9	PCIE3_RX1_P	-	NC	-	NC
3	10	PCIE3_RX1_M	-	NC	-	NC
3	11	PCIE3_TX1_P	-	NC	-	NC
3	12	PCIE3_TX1_M	-	NC	-	NC
3	13	PCIE3_RX2_P	-	NC	-	NC
3	14	PCIE3_RX2_M	-	NC	-	NC
3	15	PCIE3_TX2_P	-	NC	-	NC
3	16	PCIE3_TX2_M	-	NC	-	NC
3	17	PCIE3_RX3_P	-	NC	-	NC
3	18	PCIE3_RX3_M	-	NC	-	NC
3	19	PCIE3_TX3_P	-	NC	-	NC
3	20	PCIE3_TX3_M	-	NC	-	NC
3	21	VA_D00	-	NC	-	NC
3	22	VA_D01	-	NC	-	NC
3	23	VA_D02	-	NC	-	NC
3	24	VA_D03	-	NC	-	NC
3	25	VA_D04	-	NC	-	NC
3	26	VA_D05	-	NC	-	NC
3	27	VA_D06	-	NC	-	NC

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Voltage	Connection in the vehicle board	Direction Vehicle-Control	Connection in the control board
3	28	VA_D07	-	NC	-	NC
3	29	VA_D08	-	NC	-	NC
3	30	VA_D09	-	NC	-	NC
3	31	VA_D10	-	NC	-	NC
3	32	VA_D11	-	NC	-	NC
3	33	VA_D12	-	NC	-	NC
3	34	VA_D13	-	NC	-	NC
3	35	VA_D14	-	NC	-	NC
3	36	VA_D15	-	NC	-	NC
3	37	VA_D16	-	NC	-	NC
3	38	VA_D17	-	NC	-	NC
3	39	VA_D18	-	NC	-	NC
3	40	VA_D19	-	NC	-	NC
3	41	GND	-	GND	-(Power pin)	GND
3	42	GND	-	GND	-(Power pin)	GND
3	43	GND	-	GND	-(Power pin)	GND
3	44	GND	-	GND	-(Power pin)	GND

1.4.2. Vehicle/Audio board interface (Standard Reference Hardware)

The schematic of Vehicle/Audio Board on standard Reference Hardware Control Board side is shown in Figure 14, Figure 15 and Figure 16, and the pin assignments and the connected terminals are listed on Table 3. This is the application using R-Car H3 for the SoC and not relevant if any other SoC is used.

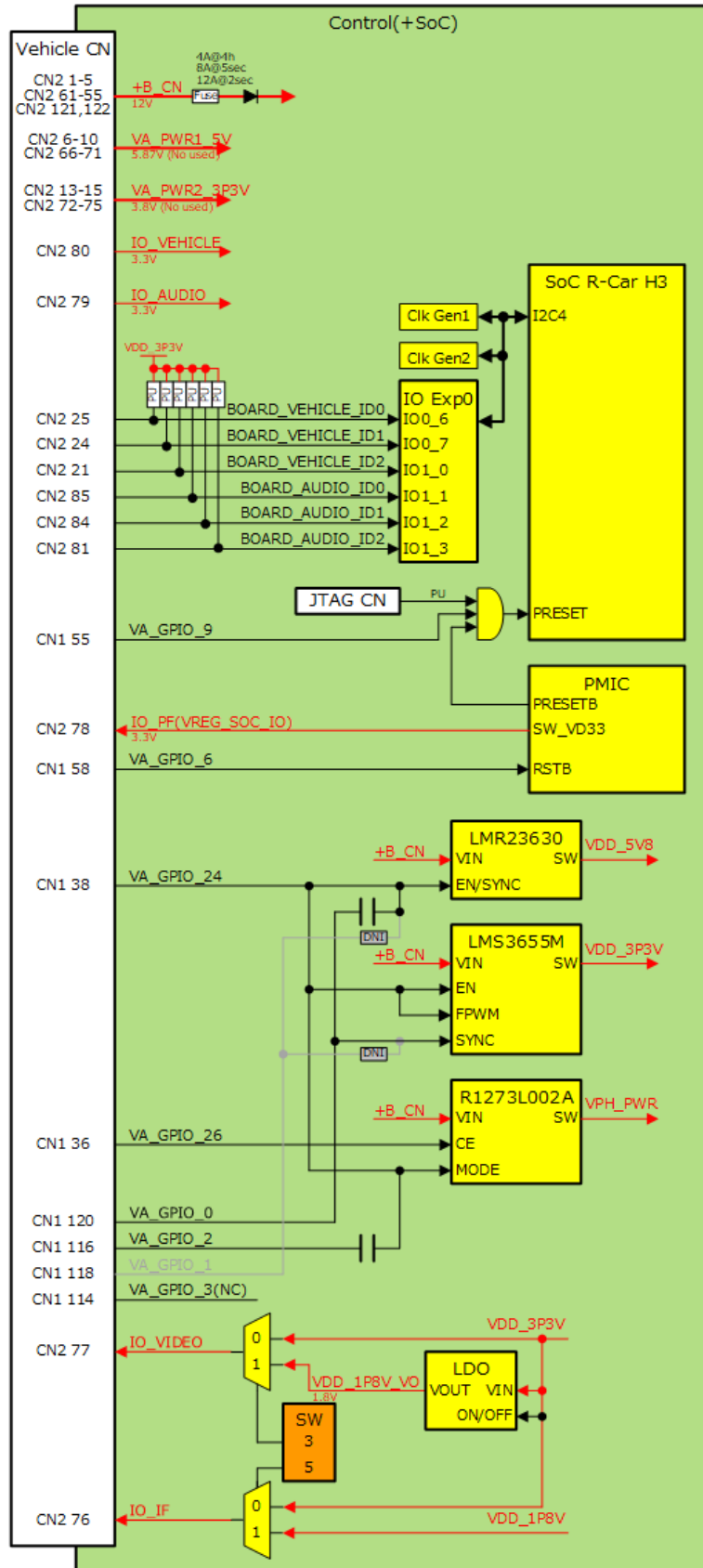


Figure 14 Connectivity between Vehicle/Audio Board and Control Board (for power supplies on standard Reference Hardware)

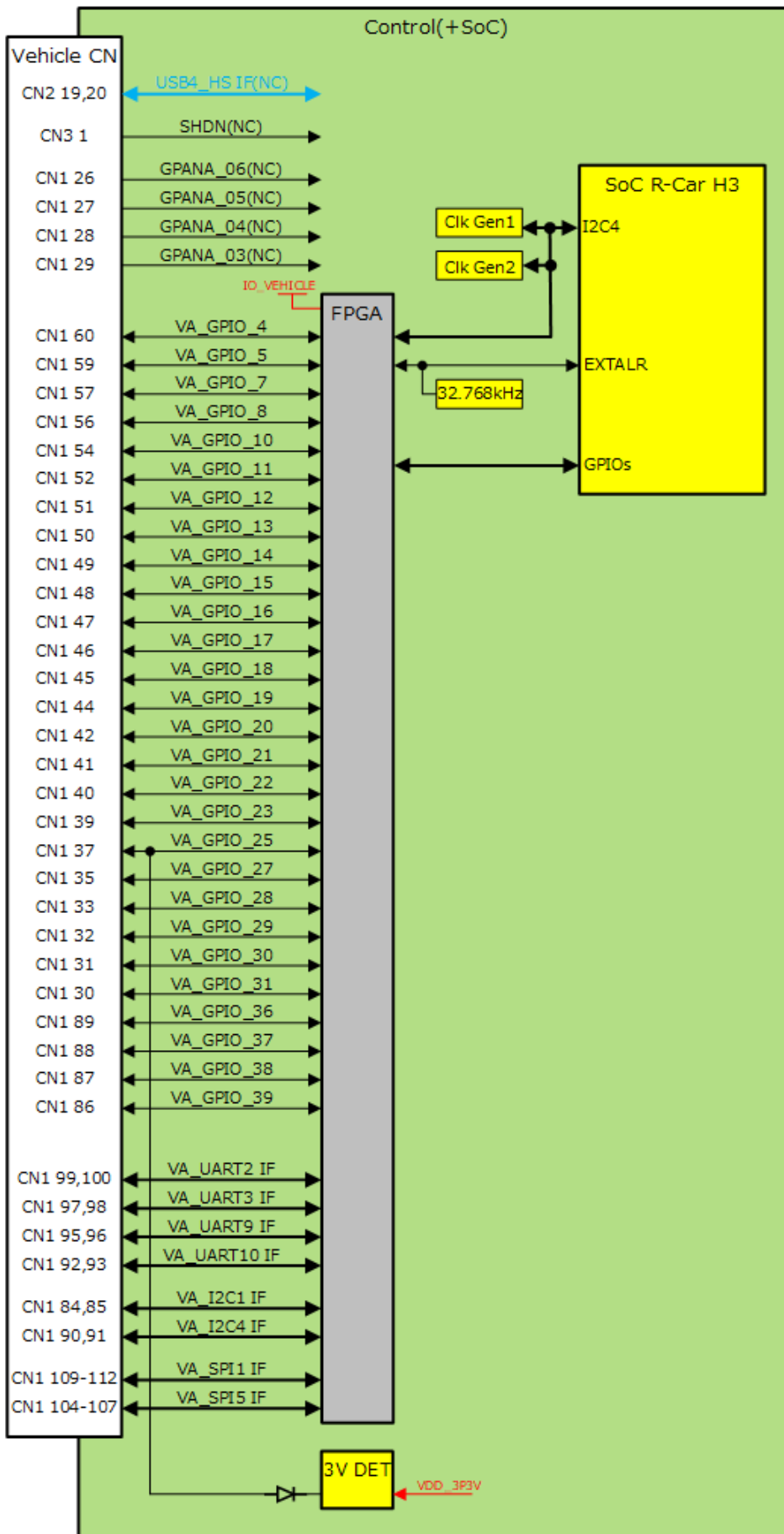


Figure 15 Connectivity between Vehicle/Audio Board and Control Board (for vehicle interfaces on standard Reference Hardware)

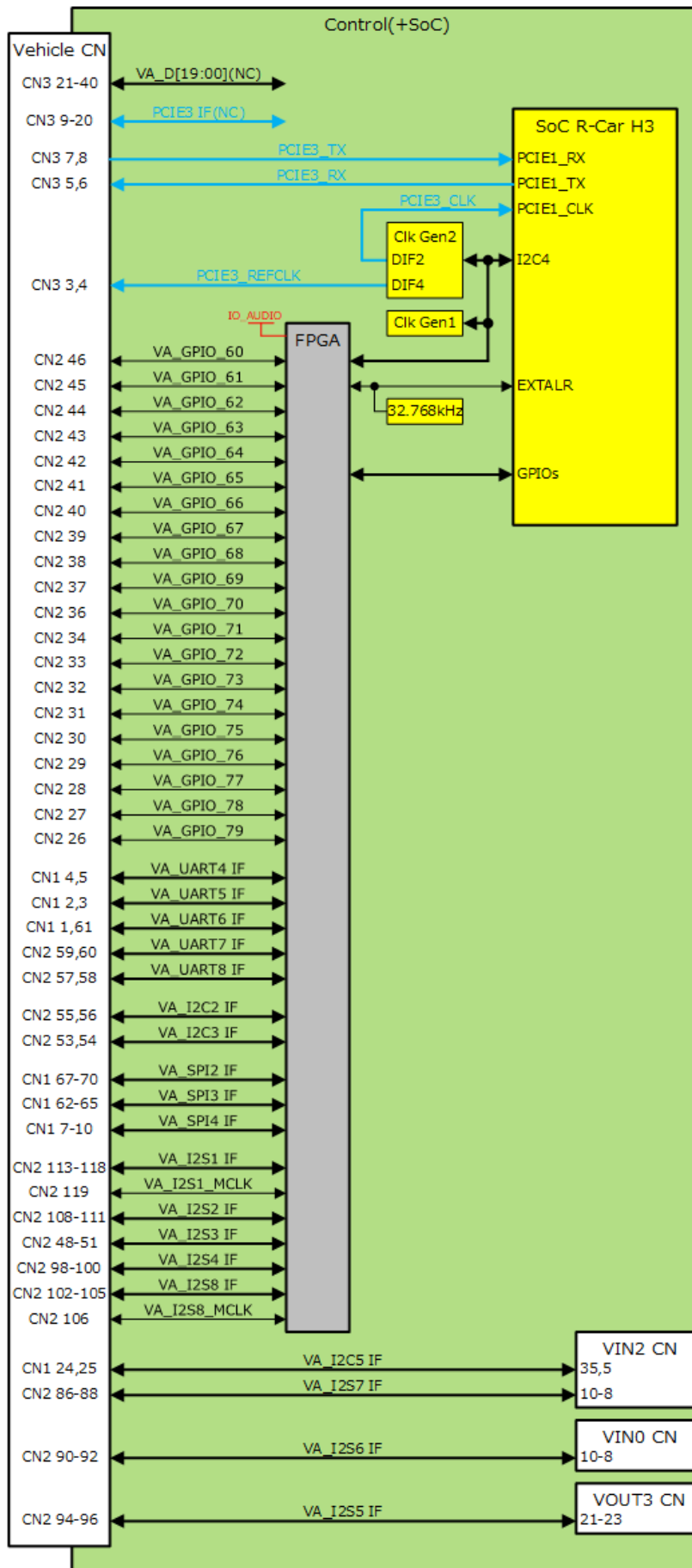


Figure 16 Connectivity between Vehicle/Audio Board and Control Board (for Audios on standard Reference Hardware)

Table 3 Connector (Vehicle/ Audio CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Refence Hardware)

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	1	VA_UART6_RX	Audio-Control	IO_AUDIO	>	FPGA	UART ch6(e.g. RS485(2)) Rx Data(SoC Rx)
1	2	VA_UART5_RX	Audio-Control	IO_AUDIO	>	FPGA	UART ch5(e.g. Tuner) Rx Data(SoC Rx)
1	3	VA_UART5_TX	Audio-Control	IO_AUDIO	<	FPGA	UART ch5(e.g. Tuner) Tx Data(SoC Tx)
1	4	VA_UART4_RX	Audio-Control	IO_AUDIO	>	FPGA	UART ch4(e.g. RS485(1)) Rx Data(SoC Rx)
1	5	VA_UART4_TX	Audio-Control	IO_AUDIO	<	FPGA	UART ch4(e.g. RS485(1)) Tx Data(SoC Tx)
1	6	GND	-	-	-	GND	GND
1	7	VA_SPI4_VAI	Audio-Control	IO_AUDIO	<	FPGA	SPI ch4(e.g. AudioCodec) Data(SoC Output)
1	8	VA_SPI4_VAO	Audio-Control	IO_AUDIO	>	FPGA	SPI ch4(e.g. AudioCodec) Data(SoC Input)
1	9	VA_SPI4_CS	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch4(e.g. AudioCodec) ChipSelect
1	10	VA_SPI4_CLK	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch4(e.g. AudioCodec) Clock
1	11	GND	-	-	-	GND	GND
1	12	GND	-	-	-	GND	GND
1	13	VA_GPIO_59	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Tuner power control1)
1	14	VA_GPIO_58	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Beep mute control)
1	15	VA_GPIO_57	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Tuner power control2)
1	16	VA_GPIO_56	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. External-amp cintrol1)
1	17	VA_GPIO_55	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. External-amp cintrol2)
1	18	VA_GPIO_54	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. External-amp cintrol3)
1	19	VA_GPIO_53	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. External-amp cintrol4)
1	20	VA_GPIO_52	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Speaker-amp mute control)
1	21	VA_GPIO_51	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Tuner power control3)

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	22	VA_GPIO_50	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Audio-out mute control)
1	23	GND	-	-	-	GND	GND
1	24	VA_I2C5_SDA	Vehicle-Audio	IO_AUDIO	<>	VideoIn2 CN 35pin	I2C ch5(e.g. AudioDSP) SDA
1	25	VA_I2C5_SCL	Vehicle-Audio	IO_AUDIO	<>	VideoIn2 CN 5pin	I2C ch5(e.g. AudioDSP) SCL
1	26	GPANA_06	Vehicle-Audio/Control	IO_VEHICLE	<>	NC	Analog signal
1	27	GPANA_05	Vehicle-Audio/Control	IO_VEHICLE	<>	NC	Analog signal
1	28	GPANA_04	Vehicle-Audio/Control	IO_VEHICLE	<>	NC	Analog signal
1	29	GPANA_03	Vehicle-Audio/Control	IO_VEHICLE	<>	NC	Analog signal
1	30	VA_GPIO_31	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	31	VA_GPIO_30	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	32	VA_GPIO_29	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	33	VA_GPIO_28	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	34	GND	-	-	-	GND	GND
1	35	VA_GPIO_27	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. Factory mode enable)
1	36	VA_GPIO_26	Vehicle-Audio/Control	IO_VEHICLE	>	DCDC(VPH_PWR) enable pin	Control-board power enable2
1	37	VA_GPIO_25	Vehicle-Control	IO_VEHICLE	<	FPGA, Voltage detect(VDD_3P3V) "OUT" pin	VDD_3P3V status
1	38	VA_GPIO_24	Vehicle-Audio/Control	IO_VEHICLE	>	DCDC(VDD_5P8V,VDD_3P3V) enable pin	Control-board power enable1
1	39	VA_GPIO_23	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	40	VA_GPIO_22	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	41	VA_GPIO_21	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	42	VA_GPIO_20	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	43	GND	-	-	-	GND	GND
1	44	VA_GPIO_19	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	45	VA_GPIO_18	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	46	VA_GPIO_17	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. Sensor interrupt1)
1	47	VA_GPIO_16	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	48	VA_GPIO_15	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	49	VA_GPIO_14	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. SoC standby request)
1	50	VA_GPIO_13	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	51	VA_GPIO_12	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	52	VA_GPIO_11	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	53	GND	-	-	-	GND	GND
1	54	VA_GPIO_10	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. SoC status1)
1	55	VA_GPIO_9	Vehicle-Control	IO_VEHICLE	>	FPGA, SoC reset input	SoC reset
1	56	VA_GPIO_8	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. SoC wakeup request)
1	57	VA_GPIO_7	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. SoC status2)
1	58	VA_GPIO_6	Vehicle-Control	IO_VEHICLE	>	FPGA, PMIC reset input	PMIC reset
1	59	VA_GPIO_5	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. SoC to Vehicle CPU interrupt)
1	60	VA_GPIO_4	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. Vehicle CPU to SoC interrupt)
1	61	VA_UART6_TX	Audio-Control	IO_AUDIO	<	FPGA	UART ch6(e.g. RS485(2)) Tx Data(SoC Tx)
1	62	VA_SPI3_VAI	Audio-Control	IO_AUDIO	<	FPGA	SPI ch3(e.g. Tuner) Data(SoC Output)
1	63	VA_SPI3_VAO	Audio-Control	IO_AUDIO	>	FPGA	SPI ch3(e.g. Tuner) Data(SoC Input)
1	64	VA_SPI3_CS	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch3(e.g. Tuner) ChipSelect
1	65	VA_SPI3_CLK	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch3(e.g. Tuner) Clock
1	66	GND	-	-	-	GND	GND
1	67	VA_SPI2_VAI	Audio-Control	IO_AUDIO	<	FPGA	SPI ch2(e.g. AudioDSP) Data(SoC Output)
1	68	VA_SPI2_VAO	Audio-Control	IO_AUDIO	>	FPGA	SPI ch2(e.g. AudioDSP) Data(SoC Input)
1	69	VA_SPI2_CS	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch2(e.g. AudioDSP) ChipSelect
1	70	VA_SPI2_CLK	Audio-Control	IO_AUDIO	<>	FPGA	SPI ch2(e.g. AudioDSP) Clock
1	71	GND	-	-	-	GND	GND
1	72	GND	-	-	-	GND	GND
1	73	VA_GPIO_49	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Speaker-amp power control)
1	74	VA_GPIO_48	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO
1	75	VA_GPIO_47	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO
1	76	VA_GPIO_46	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	77	VA_GPIO_45	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Audio-block power control1)
1	78	VA_GPIO_44	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Audio-block power control2)
1	79	VA_GPIO_43	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. AudioDSP power control)
1	80	VA_GPIO_42	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. AudioDSP mute control)
1	81	VA_GPIO_41	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. AudioDSP interrupt)
1	82	VA_GPIO_40	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. AudioDSP reset)
1	83	GND	-	-	-	GND	GND
1	84	VA_I2C1_SDA	Vehicle-Audio/Control	IO_VEHICLE	<>	FPGA, Pull-up	I2C ch1(e.g. Sensor) SDA
1	85	VA_I2C1_SCL	Vehicle-Audio/Control	IO_VEHICLE	<>	FPGA, Pull-up	I2C ch1(e.g. Sensor) SCL
1	86	VA_GPIO_39	Vehicle-Audio/Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. Sensor reset/enable)
1	87	VA_GPIO_38	Vehicle-Audio/Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. Sensor interrupt2)
1	88	VA_GPIO_37	Vehicle-Audio/Control	IO_VEHICLE	<>	FPGA	GPIO(e.g. LIN transceiver sleep mode)
1	89	VA_GPIO_36	Vehicle-Control	IO_VEHICLE	<>	FPGA	GPIO
1	90	VA_I2C4_SDA	Vehicle-Control	IO_VEHICLE	<>	FPGA	I2C ch4 SDA
1	91	VA_I2C4_SCL	Vehicle-Control	IO_VEHICLE	<>	FPGA	I2C ch4 SCL
1	92	VA_UART10_RX	Vehicle-Control	IO_VEHICLE	>	FPGA	UART ch10(e.g. LIN) Rx Data(SoC Rx)
1	93	VA_UART10_TX	Vehicle-Control	IO_VEHICLE	<	FPGA	UART ch10(e.g. LIN) Tx Data(SoC Tx)
1	94	GND	-	-	-	GND	GND
1	95	VA_UART9_RX	Vehicle-Audio/Control	IO_VEHICLE	>	FPGA	UART ch9 Rx Data(SoC Rx)
1	96	VA_UART9_TX	Vehicle-Audio/Control	IO_VEHICLE	<	FPGA	UART ch9 Tx Data(SoC Tx)
1	97	VA_UART3_RX	Vehicle-Control	IO_VEHICLE	>	FPGA	UART ch3(e.g. CAN(1)) Rx Data(SoC Rx)
1	98	VA_UART3_TX	Vehicle-Control	IO_VEHICLE	<	FPGA	UART ch3(e.g. CAN(1)) Tx Data(SoC Tx)
1	99	VA_UART2_RX	Vehicle-Control	IO_VEHICLE	>	FPGA	UART ch2(e.g. CAN(2)) Rx Data(SoC Rx)
1	100	VA_UART2_TX	Vehicle-Control	IO_VEHICLE	<	FPGA	UART ch2(e.g. CAN(2)) Tx Data(SoC Tx)

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	101	VA_UART1_RX	Vehicle-Control	IO_VEHICLE	>	FPGA	UART ch1(e.g. SoC-Vehicle CPU communication) Rx Data(SoC Rx)
1	102	VA_UART1_TX	Vehicle-Control	IO_VEHICLE	<	FPGA	UART ch1(e.g. SoC-Vehicle CPU communication) Tx Data(SoC Tx)
1	103	GND	-	-	-	GND	GND
1	104	VA_SPI5_VAI	Vehicle-Control	IO_VEHICLE	<	FPGA	SPI ch5 Data(SoC Output)
1	105	VA_SPI5_VAO	Vehicle-Control	IO_VEHICLE	>	FPGA	SPI ch5 Data(SoC Input)
1	106	VA_SPI5_CS	Vehicle-Control	IO_VEHICLE	<>	FPGA	SPI ch5 ChipSelect
1	107	VA_SPI5_CLK	Vehicle-Control	IO_VEHICLE	<>	FPGA	SPI ch5 Clock
1	108	GND	-	-	-	GND	GND
1	109	VA_SPI1_VAI	Vehicle-Control	IO_VEHICLE	<	FPGA	SPI ch1(e.g. SoC-Vehicle CPU communication) Data(SoC Output)
1	110	VA_SPI1_VAO	Vehicle-Control	IO_VEHICLE	>	FPGA	SPI ch1(e.g. SoC-Vehicle CPU communication) Data(Soc Input)
1	111	VA_SPI1_CS	Vehicle-Control	IO_VEHICLE	<>	FPGA	SPI ch1(e.g. SoC-Vehicle CPU communication) ChipSelect
1	112	VA_SPI1_CLK	Vehicle-Control	IO_VEHICLE	<>	FPGA	SPI ch1(e.g. SoC-Vehicle CPU communication) Clock
1	113	GND	-	-	-	GND	GND
1	114	VA_GPIO_3	Vehicle-Audio	IO_VEHICLE	<>	NC	Vehicle/Audio signal GPIO(e.g. Tuner power control3)
1	115	GND	-	-	-	GND	GND
1	116	VA_GPIO_2	Vehicle-Audio/Control	IO_VEHICLE	>	DCDC(R1273L(VPH_PWR)) "MODE" pin (sync clock)	DCDC(VPH_PWR) switching synchronous clock
1	117	GND	-	-	-	GND	GND
1	118	VA_GPIO_1	Vehicle-Audio/Control	IO_VEHICLE	>	No used	-
1	119	GND	-	-	-	GND	GND
1	120	VA_GPIO_0	Vehicle-Audio/Control	IO_VEHICLE	>	DCDC(LMS3655(VDD_3P3V)) "SYNC" pin, DCDC(LMR23630(VDD_5P8V)) "EN/SYNC" pin	DCDC(VDD_3P3V,VDD_5P8V) switching synchronous clock
1	121	GND	-	-	- (Power pin)	GND	GND
1	122	GND	-	-	- (Power pin)	GND	GND
1	123	GND	-	-	- (Power pin)	GND	GND

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
1	124	GND	-	-	- (Power pin)	GND	GND
2	1	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	2	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	3	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	4	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	5	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	6	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	7	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	8	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	9	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	10	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	11	Reserved	-	-	-	NC	Reserved pin for power
2	12	Reserved	-	-	-	NC	Reserved pin for power
2	13	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	14	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	15	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	16	Reserved	-	-	-	NC	Reserved pin for power
2	17	Reserved	-	-	-	NC	Reserved pin for signal
2	18	Reserved	-	-	-	NC	Reserved pin for signal
2	19	USB4_D_M	Vehicle/Audio-Control	LVDS	<>	NC	USB ch4 Data-
2	20	USB4_D_P	Vehicle/Audio-Control	LVDS	<>	NC	USB ch4 Data+
2	21	BOARD_VEHICLE_ID2	Vehicle-Control	3.3[V]	>	IO Expander(PC9539)-0 "IO1_0" pin, Pull-up	Vehicle Board ID bit2
2	22	GND	-	-	-	GND	GND
2	23	GND	-	-	-	GND	GND
2	24	BOARD_VEHICLE_ID1	Vehicle-Control	3.3[V]	>	IO Expander(PC9539)-0 "IO0_7" pin, Pull-up	Vehicle Board ID bit1
2	25	BOARD_VEHICLE_ID0	Vehicle-Control	3.3[V]	>	IO Expander(PC9539)-0 "IO0_6" pin, Pull-up	Vehicle Board ID bit0
2	26	VA_GPIO_79	Audio-Control	IO_AUDIO	<>	FPGA	Audio power enable
2	27	VA_GPIO_78	Audio-Control	IO_AUDIO	<>	FPGA	External power supply enable1

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
2	28	VA_GPIO_77	Audio-Control	IO_AUDIO	<>	FPGA	External power supply enable2
2	29	VA_GPIO_76	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. AudioCodec power-down)
2	30	VA_GPIO_75	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. RS485(2) transceiver driver output enable)
2	31	VA_GPIO_74	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. RS485(2) transceiver receiver output enable)
2	32	VA_GPIO_73	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	33	VA_GPIO_72	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	34	VA_GPIO_71	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	35	GND	-	-	-	GND	GND
2	36	VA_GPIO_70	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	37	VA_GPIO_69	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	38	VA_GPIO_68	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. CAN(1) transceiver standby mode)
2	39	VA_GPIO_67	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. CAN(2) transceiver standby mode)
2	40	VA_GPIO_66	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. IEBus transceiver standby mode)
2	41	VA_GPIO_65	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. RS485(1) transceiver driver output enable)
2	42	VA_GPIO_64	Audio-Control	IO_AUDIO	<>	FPGA	GPIO(e.g. RS485(1) transceiver receiver output enable)
2	43	VA_GPIO_63	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	44	VA_GPIO_62	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	45	VA_GPIO_61	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	46	VA_GPIO_60	Audio-Control	IO_AUDIO	<>	FPGA	GPIO
2	47	GND	-	-	-	GND	GND
2	48	VA_I2S3_DATA1	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch3(secondary audio out) Data1
2	49	VA_I2S3_DATA0	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch3(secondary audio out) Data0
2	50	VA_I2S3_LRCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch3(secondary audio out) LR Clock
2	51	VA_I2S3_BCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch3(secondary audio out) Bit Clock
2	52	GND	-	-	-	GND	GND
2	53	VA_I2C3_SDA	Audio-Control	IO_AUDIO	<>	FPGA	I2C ch3 SDA
2	54	VA_I2C3_SCL	Audio-Control	IO_AUDIO	<>	FPGA	I2C ch3 SCL
2	55	VA_I2C2_SDA	Audio-Control	IO_AUDIO	<>	FPGA	I2C ch2(e.g. AudioCodec) SDA

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
2	56	VA_I2C2_SCL	Audio-Control	IO_AUDIO	<>	FPGA	I2C ch2(e.g. AudioCodec) SCL
2	57	VA_UART8_RX	Audio-Control	IO_AUDIO	>	FPGA	UART ch8(e.g. IEBus) Rx Data(SoC Rx)
2	58	VA_UART8_TX	Audio-Control	IO_AUDIO	<	FPGA	UART ch8(e.g. IEBus) Tx Data(SoC Tx)
2	59	VA_UART7_RX	Audio-Control	IO_AUDIO	>	FPGA	UART ch7 Rx Data(SoC Rx)
2	60	VA_UART7_TX	Audio-Control	IO_AUDIO	<	FPGA	UART ch7 Tx Data(SoC Tx)
2	61	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	62	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	63	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	64	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	65	+B_CN	Vehicle-Audio/Control	12[V]	>	DCDCs/LDOs VIN	Power input from vehicle
2	66	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	67	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	68	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	69	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	70	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	71	VA_PWR1_5V	Vehicle-Audio/Control	5.87[V]	>	No used	Common 5.8[V] power
2	72	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	73	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	74	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	75	VA_PWR2_3P3V	Vehicle-Audio/Control	3.8V	>	No used	Common 3.8[V] power
2	76	IO_IF	Vehicle/Audio-Control	3.3[V]	<	LDO VOUT(VDD_USB_IOBANK)	IO power for USB IO
2	77	IO_VIDEO	Vehicle/Audio-Control	3.3[V]	<	LDO VOUT(VDD_VOUT_IOBANK)	IO power for VideoOut IO
2	78	IO_PF	Vehicle/Audio-Control	3.3[V]	<	PMIC VOUT(VREG_SOC_IO)	IO power for SoC IO
2	79	IO_AUDIO	Audio-Control	3.3[V]	>	Level shifter VCC	IO power for Audio IO
2	80	IO_VEHICLE	Vehicle-Audio/Control	3.3[V]	>	Level shifter VCC	IO power for Vehicle IO
2	81	BOARD_AUDIO_ID2	Audio-Control	3.3[V]	>	IO Expander(PC9539)-0 "IO1_3" pin, Pull-up	Audio Board ID bit2
2	82	GND	-	-	-	GND	GND
2	83	GND	-	-	-	GND	GND
2	84	BOARD_AUDIO_ID1	Audio-Control	3.3[V]	>	IO Expander(PC9539)-0 "IO1_2" pin, Pull-up	Audio Board ID bit1

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
2	85	BOARD_AUDIO_ID0	Audio-Control	3.3[V]	>	IO Expander(PCA9539)-0 "IO1_1" pin, Pull-up	Audio Board ID bit0
2	86	VA_I2S7_DATA	Audio-Control	IO_AUDIO	<>	VideoIn2 CN 10pin	I2S ch7(VideoIn2) Data
2	87	VA_I2S7_LRCLK	Audio-Control	IO_AUDIO	<>	VideoIn2 CN 9pin	I2S ch7(VideoIn2) LR Clock
2	88	VA_I2S7_BCLK	Audio-Control	IO_AUDIO	<>	VideoIn2 CN 8pin	I2S ch7(VideoIn2) Bit Clock
2	89	GND	-	-	-	GND	GND
2	90	VA_I2S6_DATA	Audio-Control	IO_AUDIO	<>	VideoIn0 CN 10pin	I2S ch6(VideoIn0) Data
2	91	VA_I2S6_LRCLK	Audio-Control	IO_AUDIO	<>	VideoIn0 CN 9pin	I2S ch6(VideoIn0) LR Clock
2	92	VA_I2S6_BCLK	Audio-Control	IO_AUDIO	<>	VideoIn0 CN 8pin	I2S ch6(VideoIn0) Bit Clock
2	93	GND	-	-	-	GND	GND
2	94	VA_I2S5_DATA	Audio-Control	IO_AUDIO	<>	VideoOut3 21pin	I2S ch5(VideoOut3) Data
2	95	VA_I2S5_LRCLK	Audio-Control	IO_AUDIO	<>	VideoOut3 22pin	I2S ch5(VideoOut3) LR Clock
2	96	VA_I2S5_BCLK	Audio-Control	IO_AUDIO	<>	VideoOut3 23pin	I2S ch5(VideoOut3) Bit Clock
2	97	GND	-	-	-	GND	GND
2	98	VA_I2S4_DATA	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch4(secondary audio in) Data
2	99	VA_I2S4_LRCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch4(secondary audio in) LR Clock
2	100	VA_I2S4_BCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch4(secondary audio in) Bit Clock
2	101	GND	-	-	-	GND	GND
2	102	VA_I2S8_DATA1	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch8 Data1
2	103	VA_I2S8_DATA0	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch8 Data0
2	104	VA_I2S8_LRCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch8 LR Clock
2	105	VA_I2S8_BCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch8 Bit Clock
2	106	VA_I2S8_MCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch8 Master Clock
2	107	GND	-	-	-	GND	GND
2	108	VA_I2S2_DATA1	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch2(primary audio in) Data1
2	109	VA_I2S2_DATA0	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch2(primary audio in) Data0
2	110	VA_I2S2_LRCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch2(primary audio in) LR Clock
2	111	VA_I2S2_BCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch2(primary audio in) Bit Clock
2	112	GND	-	-	-	GND	GND
2	113	VA_I2S1_DATA3	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Data3
2	114	VA_I2S1_DATA2	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Data2

Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
2	115	VA_I2S1_DATA1	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Data1
2	116	VA_I2S1_DATA0	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Data0
2	117	VA_I2S1_LRCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) LR Clock
2	118	VA_I2S1_BCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Bit Clock
2	119	VA_I2S1_MCLK	Audio-Control	IO_AUDIO	<>	FPGA	I2S ch1(primary audio out/in) Master Clock
2	120	Reserved	-	-	-	NC	Reserved pin for signal
2	121	+B_CN	Vehicle-Audio/Control	12[V]	> (Power pin)	DCDCs/LDOs VIN	Power input from vehicle
2	122	GND	-	-	- (Power pin)	GND	GND
2	123	+B_CN	Vehicle-Audio/Control	12[V]	> (Power pin)	DCDCs/LDOs VIN	Power input from vehicle
2	124	GND	-	-	- (Power pin)	GND	GND
3	1	SHDN	Audio-Control	IO_VEHICLE	-	NC	SoC shut down request
3	2	GND	-	-	-	GND	GND
3	3	PCIE3_REFCLK_P	Vehicle/Audio-Control	LVDS	<	SoC PCIe ch3 REFCLK+	PCIe ch3 REFCLK+
3	4	PCIE3_REFCLK_M	Vehicle/Audio-Control	LVDS	<	SoC PCIe ch3 REFCLK-	PCIe ch3 REFCLK-
3	5	PCIE3_RX0_P	Vehicle/Audio-Control	LVDS	<	SoC PCIe ch3 Tx Data+(SoC Tx)	PCIe ch3 Rx0 Data+(SoC Tx)
3	6	PCIE3_RX0_M	Vehicle/Audio-Control	LVDS	<	SoC PCIe ch3 Tx Data-(SoC Tx)	PCIe ch3 Rx0 Data-(SoC Tx)
3	7	PCIE3_TX0_P	Vehicle/Audio-Control	LVDS	>	SoC PCIe ch3 Rx Data+(SoC Rx)	PCIe ch3 Tx0 Data+(SoC Rx)
3	8	PCIE3_TX0_M	Vehicle/Audio-Control	LVDS	>	SoC PCIe ch3 Rx Data-(SoC Rx)	PCIe ch3 Tx0 Data-(SoC Rx)
3	9	PCIE3_RX1_P	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx1 Data+(SoC Tx)
3	10	PCIE3_RX1_M	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx1 Data-(SoC Tx)
3	11	PCIE3_TX1_P	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx1 Data+(SoC Rx)
3	12	PCIE3_TX1_M	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx1 Data-(SoC Rx)
3	13	PCIE3_RX2_P	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx2 Data+(SoC Tx)
3	14	PCIE3_RX2_M	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx2 Data-(SoC Tx)
3	15	PCIE3_TX2_P	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx2 Data+(SoC Rx)
3	16	PCIE3_TX2_M	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx2 Data-(SoC Rx)
3	17	PCIE3_RX3_P	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx3 Data+(SoC Tx)
3	18	PCIE3_RX3_M	Vehicle/Audio-Control	LVDS	<	NC	PCIe ch3 Rx3 Data-(SoC Tx)

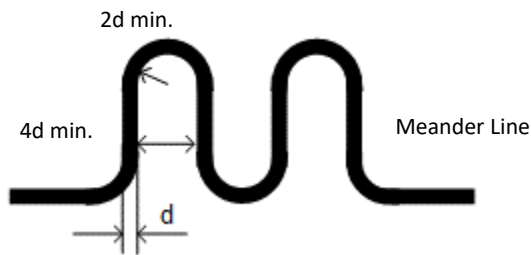
Reference Hardware Design Guideline for Vehicle/Audio Board

CN	Pin	Signal Name	Assumed use block	Voltage	Direction Vehicle-Control	Connection in the control board	Description Example of use
3	19	PCIE3_TX3_P	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx3 Data+(SoC Rx)
3	20	PCIE3_TX3_M	Vehicle/Audio-Control	LVDS	>	NC	PCIe ch3 Tx3 Data-(SoC Rx)
3	21	VA_D00	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit0
3	22	VA_D01	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit1
3	23	VA_D02	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit2
3	24	VA_D03	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit3
3	25	VA_D04	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit4
3	26	VA_D05	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit5
3	27	VA_D06	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit6
3	28	VA_D07	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit7
3	29	VA_D08	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit8
3	30	VA_D09	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit9
3	31	VA_D10	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit10
3	32	VA_D11	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit11
3	33	VA_D12	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit12
3	34	VA_D13	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit13
3	35	VA_D14	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit14
3	36	VA_D15	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit15
3	37	VA_D16	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit16
3	38	VA_D17	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit17
3	39	VA_D18	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit18
3	40	VA_D19	Vehicle/Audio-Control	IO_PF	<>	NC	CMOS Bus bit19
3	41	GND	-	-	- (Power pin)	GND	GND
3	42	GND	-	-	- (Power pin)	GND	GND
3	43	GND	-	-	- (Power pin)	GND	GND
3	44	GND	-	-	- (Power pin)	GND	GND

1.5. Board Layout Consideration

PCI-Express differential signal

- Trace Length Matching: Difference between a differential signal pair (+and –) must be 0.1[mm] maximum.
- Difference between an average length of a clock pair (average of + signal and – signal)/a data signal pair : 0.1[mm] maximum.
- Maximum Trace Length: 60[mm]
- Differential Impedance : 85[Ω](85[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be at least twice the width of the trace. The gap between the meander traces should be at least four times the trace width.



USB-High-speed Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and -) must be 0.5[mm] maximum.
- Maximum Trace length : 200[mm]
- Differential Impedance : 90[Ω](90[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be at least twice the width of the trace. The gap between the meander traces should be at least four times the trace width. (as shown above)

CMOS Bus Signals

- Length gap between the clock signal trace and data/command signal trace : 1.0[mm] or less for frequency of 20[MHz] or above. 5.0[mm] for 20[MHz] or less.
- Signals lines are to be gathered to make a bus signal.
A bus consisting of a set of signals should be shielded (GND trace width at least 0.1[mm]) horizontally and vertically.

Clock Signals

- Comply with line impedance requirement if specified.
- Minimize trace length and create routing with minimal divergence possible.
Shield the signals (GND trace width at least 0.1[mm]) horizontally and vertically

Analog Signals

- Comply with line impedance requirement if specified.
- Shield the signals (GND trace width at least 0.1[mm]) horizontally and vertically
A pair of + and – signals should be shielded together (GND trace width at least 0.1[mm]) horizontally and vertically

Power Supply

- Comply with power supply requirements (impedance property, etc.) of the device to connect.
If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[°C] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.

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