Reference Hardware Design Guideline

VideoOut Board

Version	Date
1.0	May 25, 2020

Panasonic Corporation

Automotive Company R&D Division

Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

References

No.	Document	Version	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

Contents

Figures and Tables

1. VideoOut Board

VideoOut Board is connected to Control board and mainly outputs images to a display, etc. There are 4 from VideoOut0 to VideoOut3 and a maximum of 4 boards can be connected to use concurrently. 1 pair of differential clock signal and 4 pairs of data signal as 1 channel (total 5 pairs=10 lines) is connected as an interface with image data from SoC.

Depending on a SoC, the signals required for image input can be also assigned to VideoOut0 and VideoOut1 to which a board for image input and output can be connected. In addition, VideoOut3 enables 24bit DPI signal connection using differential signal lines.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

1.1. Board Outline

The following figure shows VideoOut Board dimension. 1.2[mm] is the assumed board thickness. If the change is required, interference with other boards should be considered.

The interface to Control Board is a 60-pin board-to-board connector mounted on the solder side of VideoOut Board. The external interface connectors are mounted on the component side so as to avoid the interference with another board when assembled.

The spacing between the board and chassis is shown as below. External interface connectors are to be placed in the position relative to the chassis.

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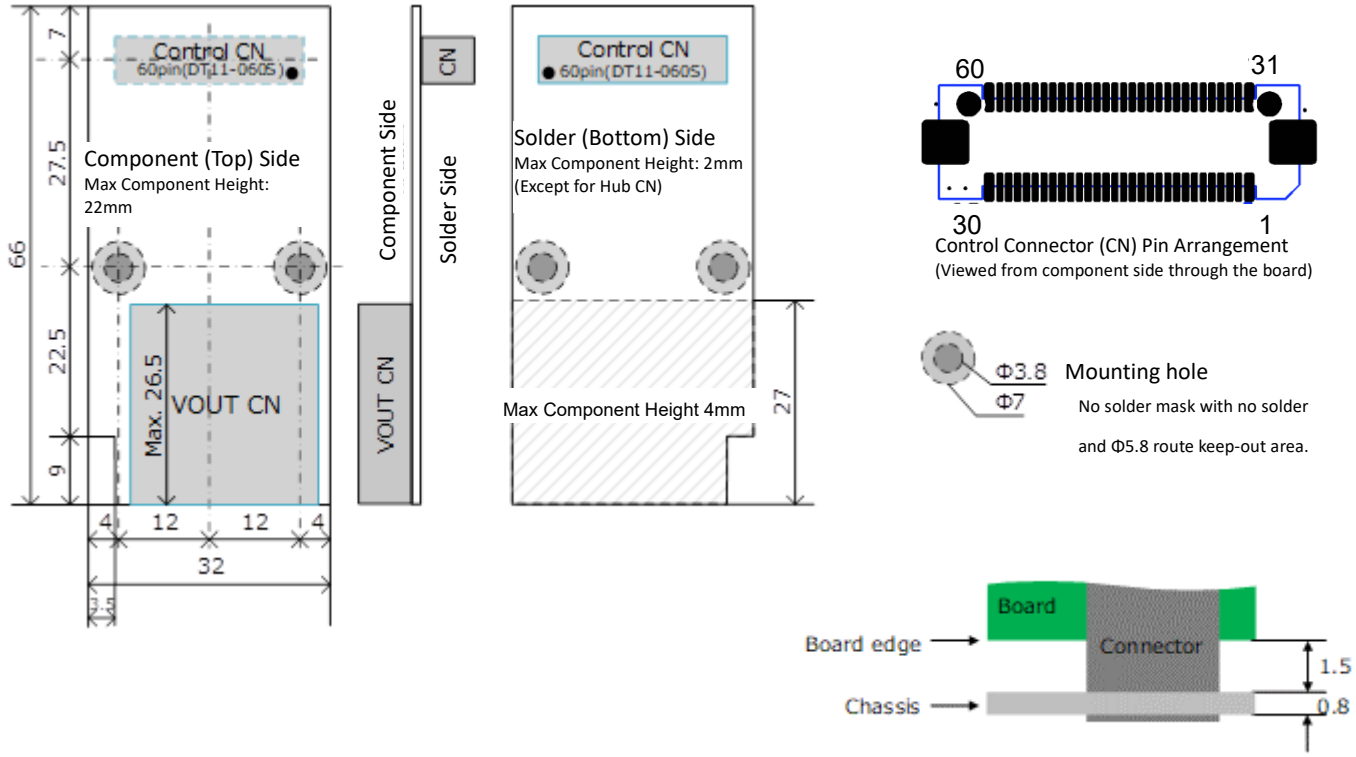


Figure 1 VideoOut Board Dimension

The space for 2 boards can be used if the space is not enough.
Either one of the following combinations is applicable.

VideoOut0 (CN1 on Figure 2) +VideoOut3 (CN2 on Figure 2)
VideoOut1 (CN1 on Figure 2) +VideoOut0 (CN2 on Figure 2)
VideoOut2 (CN1 on Figure 2) +VideoOut1 (CN2 on Figure 2)

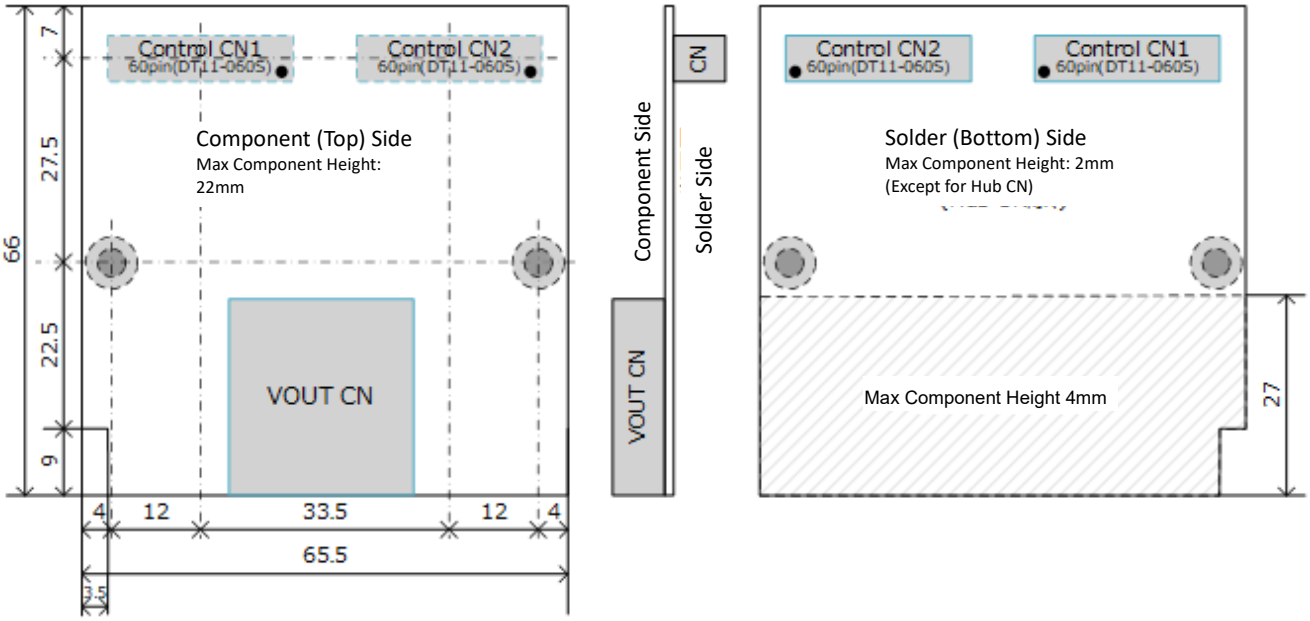


Figure 2 VideoOut Expanded Board Dimension

1.2. Power Supply

VideoOut board is provided with the following 4 lines of power supply. Each power supply is specified as below.

Table 1 VideoOut Board Power Supply

Power Supply Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
VDD_5P8V		5.87		200	Pin 29, Pin 30 (2 pins)
VDD_3P3V		3.3		200	Pin 59, Pin 60 (2 pins)
VDD_1P8V		1.8		200	Pin 27, Pin 28 (2 pins)
VDD_VOUT_CORE		1.2/1.5		150	Pin 57, Pin 58 (2 pins) Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board. The voltages of all the four lines, VideoOut0-3, are changed when setting the switch. 1.5V is the default setting for R-Car H3 Reference Hardware

A power circuit can be built on VideoOut Board if no power source is available for an intended purpose.
Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, it is possible to supplement the amount with another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards), or expanding the board is also another option so that power supply is available from two connectors. Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins.

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

1.3. Board-to-Board Interface

60-pin board-to-board connectors is used to connect Control Board to VideoOut Board. A receptacle connector (KEL DT01-060S) is assumed to be used on the side of Control board and a plug connector (KEL DT11-060S-10) is assumed to be used on the side of VideoOut board.
These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of ±0.5 [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA]

Either 1.8[V] or 3.3[V] should be applied for signals interfacing with Control board as there are a variety of boards might be used for VideoOut Board simultaneously. The voltage applied to the signals should be able to manage to a consistent level using a level shifter. When a signal output is on VideoOut side, and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.
A pull-up or pull-down resistor should be added to VideoOut Board for the external resistor required for I2C signal, etc.

1.3.1. VideoOut0 Board Interface (R-Car H3 Reference Hardware)

Figure 3 shows a schematic illustrating simplified connections between Control Board and VideoOut0 Board in R-Car H3 Reference Hardware. Connector (VOUT0 CN) pin assignments and connected terminals are listed on Table 2.

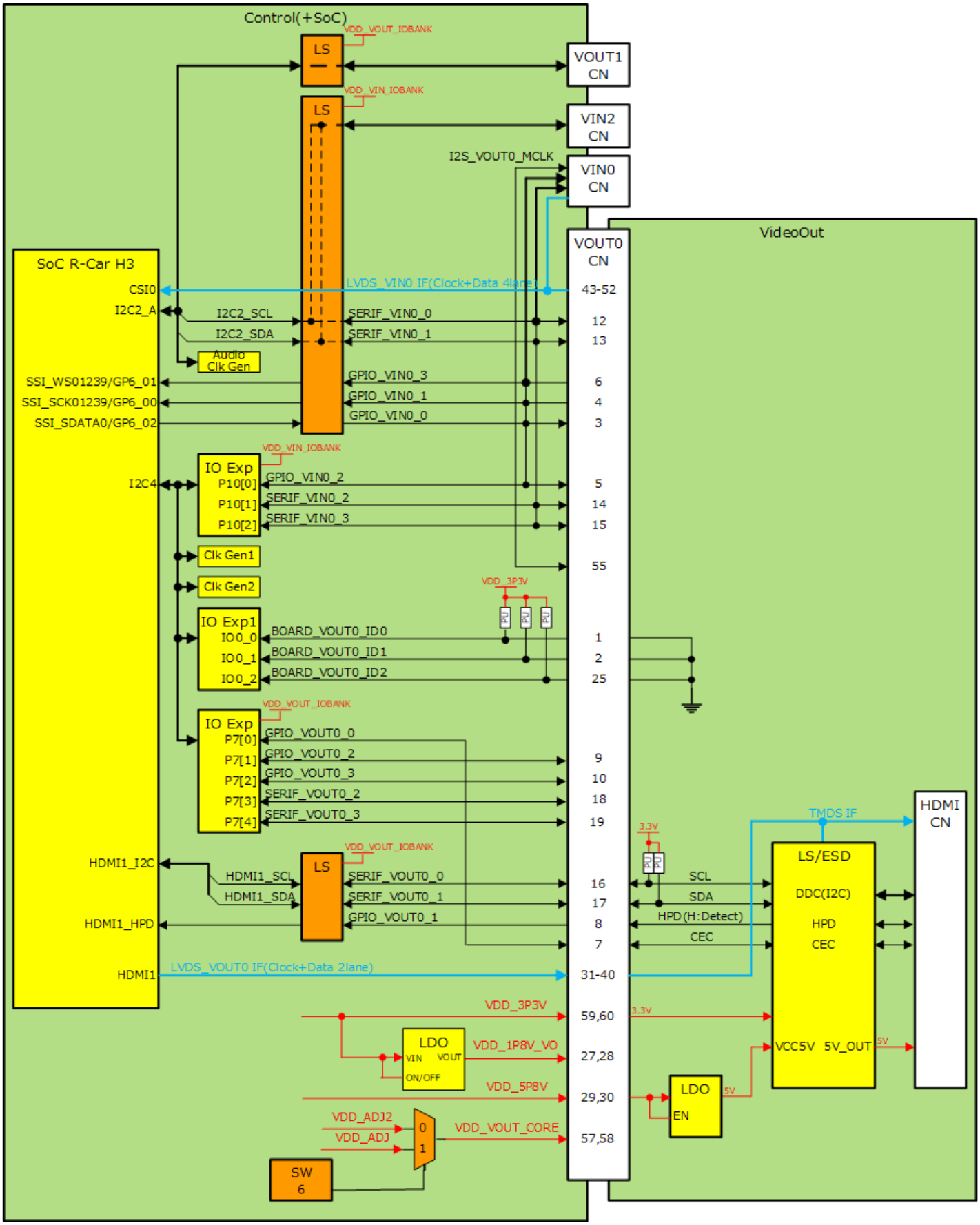


Figure 3 Connectivity between VideoOut0 Board and Control Board (R-Car H3 Reference Hardware)

Table 2 Connector (VOUT0 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control – VOUT0	Voltage	Connection of the control board	Description
31	LVDS_OUT0_CLK_P	>	LVDS	R-Car H3 "HDMI1_TMDSCLKP" pin	HDMI ch1 TMDS Clock+
32	LVDS_OUT0_CLK_M	>	LVDS	R-Car H3 "HDMI1_TMDSCLKN" pin	HDMI ch1 TMDS Clock-
33	LVDS_OUT0_LN0_P	>	LVDS	R-Car H3 "HDMI1_TMDSDATAP0" pin	HDMI ch1 TMDS Data0+
34	LVDS_OUT0_LN0_M	>	LVDS	R-Car H3 "HDMI1_TMDSDATAN0" pin	HDMI ch1 TMDS Data0-
35	LVDS_OUT0_LN1_P	>	LVDS	R-Car H3 "HDMI1_TMDSDATAP1" pin	HDMI ch1 TMDS Data1+
36	LVDS_OUT0_LN1_M	>	LVDS	R-Car H3 "HDMI1_TMDSDATAN1" pin	HDMI ch1 TMDS Data1-
37	LVDS_OUT0_LN2_P	>	LVDS	R-Car H3 "HDMI1_TMDSDATAP2" pin	HDMI ch1 TMDS Data2+
38	LVDS_OUT0_LN2_M	>	LVDS	R-Car H3 "HDMI1_TMDSDATAN2" pin	HDMI ch1 TMDS Data2-
39	LVDS_OUT0_LN3_P	-	-	NC	-
40	LVDS_OUT0_LN3_M	-	-	NC	-
43	LVDS_IN0_CLK_P	<	LVDS	R-Car H3 "CSI0_CLKP" pin	No used
44	LVDS_IN0_CLK_M	<	LVDS	R-Car H3 "CSI0_CLKN" pin	No used
45	LVDS_IN0_LN0_P	<	LVDS	R-Car H3 "CSI0_DATAP0" pin	No used
46	LVDS_IN0_LN0_M	<	LVDS	R-Car H3 "CSI0_DATAN0" pin	No used
47	LVDS_IN0_LN1_P	<	LVDS	R-Car H3 "CSI0_DATAP1" pin	No used
48	LVDS_IN0_LN1_M	<	LVDS	R-Car H3 "CSI0_DATAN1" pin	No used
49	LVDS_IN0_LN2_P	<	LVDS	R-Car H3 "CSI0_DATAP2" pin	No used
50	LVDS_IN0_LN2_M	<	LVDS	R-Car H3 "CSI0_DATAN2" pin	No used
51	LVDS_IN0_LN3_P	<	LVDS	R-Car H3 "CSI0_DATAP3" pin	No used
52	LVDS_IN0_LN3_M	<	LVDS	R-Car H3 "CSI0_DATAN3" pin	No used
7	GPIO_VOUT0_0	<>	3.3[V] *2	IO Expander-7 bit0	No used
8	GPIO_VOUT0_1	<	3.3[V] *2	R-Car H3 "HDMI1_HPD" pin	HDMI ch1 Hot plug detect
9	GPIO_VOUT0_2	<>	3.3[V] *2	IO Expander-7 bit1	No used
10	GPIO_VOUT0_3	<>	3.3[V] *2	IO Expander-7 bit2	No used
3	GPIO_VIN0_0	>	3.3[V] *3	R-Car H3 "SSI_SDATA0/GP6_02" pin	No used
4	GPIO_VIN0_1	<	3.3[V] *3	R-Car H3 "SSI_SCK01239/GP6_00" pin	No used
5	GPIO_VIN0_2	<>	3.3[V] *3	IO Expander-10 bit0	No used
6	GPIO_VIN0_3	>	3.3[V] *3	R-Car H3 "SSI_WS01239/GP6_01" pin	No used

Pin	Signal Name	Direction Control – VOUT0	Voltage	Connection of the control board	Description
16	SERIF_VOUT0_0	<>	3.3[V] *2	R-Car H3 "HDMI1_SCL" pin	HDMI ch1 DDC SCL
17	SERIF_VOUT0_1	<>	3.3[V] *2	R-Car H3 "HDMI1_SDA" pin	HDMI ch1 DDC SDA
18	SERIF_VOUT0_2	<>	3.3[V] *2	IO Expander-7 bit3	No used
19	SERIF_VOUT0_3	<>	3.3[V] *2	IO Expander-7 bit4	No used
12	SERIF_VIN0_0	<>	3.3[V] *3	R-Car H3 "RTS0#/SCL2_A" pin	No used
13	SERIF_VIN0_1	<>	3.3[V] *3	R-Car H3 "SCK0/SDA2_A" pin	No used
14	SERIF_VIN0_2	<>	3.3[V] *3	IO Expander-10 bit1	No used
15	SERIF_VIN0_3	<>	3.3[V] *3	IO Expander-10 bit2	No used
21	I2S_VOUT0_DATA	-	-	No used	-
22	I2S_VOUT0_LRCLK	-	-	No used	-
23	I2S_VOUT0_BCLK	-	-	No used	-
55	I2S_VOUT0_MCLK	-	-	No used	-
1	BOARD_VOUT0_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_0" pin, Pull-up	VideoOut0 Board ID bit0
2	BOARD_VOUT0_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_1" pin, Pull-up	VideoOut0 Board ID bit1
25	BOARD_VOUT0_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_2" pin, Pull-up	VideoOut0 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control – VOUT0	Voltage	Connection of the control board	Description
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VOUT IO voltage) on Control Board
*3: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control board

1.3.2. VideoOut0 Board Interface (Standard Reference Hardware)

Figure 4 shows a schematic of Control Board with VOUT0 CN that connects to VideoOut0 Board in StandardReference Hardware. Pin assignments of the connector (VOUT0 CN) and connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

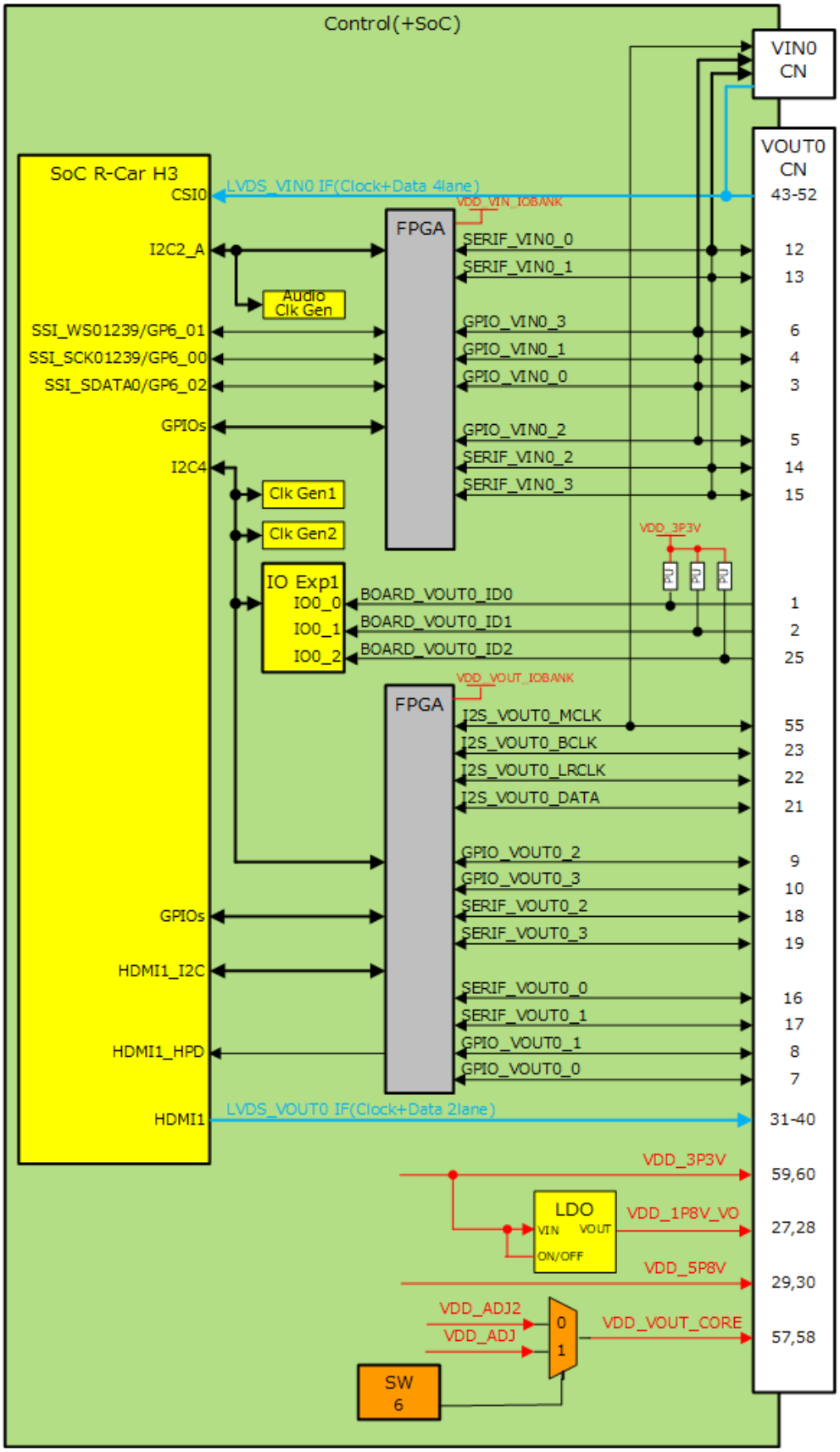


Figure 4 Connectivity between VideoOut0 Board and Control Board (Standard Reference Hardware)

Table 3 Connector (VOUT0 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VOUT0	Voltage	Connection of the control board	Description Example of use
31	LVDS_OUT0_CLK_P	>	LVDS	SoC VideoOut LVDS ch0 Clock+	SoC VideoOut LVDS ch0 Clock+
32	LVDS_OUT0_CLK_M	>	LVDS	SoC VideoOut LVDS ch0 Clock-	SoC VideoOut LVDS ch0 Clock-
33	LVDS_OUT0_LN0_P	>	LVDS	SoC VideoOut LVDS ch0 Data0+	SoC VideoOut LVDS ch0 Data0+
34	LVDS_OUT0_LN0_M	>	LVDS	SoC VideoOut LVDS ch0 Data0-	SoC VideoOut LVDS ch0 Data0-
35	LVDS_OUT0_LN1_P	>	LVDS	SoC VideoOut LVDS ch0 Data1+	SoC VideoOut LVDS ch0 Data1+
36	LVDS_OUT0_LN1_M	>	LVDS	SoC VideoOut LVDS ch0 Data1-	SoC VideoOut LVDS ch0 Data1-
37	LVDS_OUT0_LN2_P	>	LVDS	SoC VideoOut LVDS ch0 Data2+	SoC VideoOut LVDS ch0 Data2+
38	LVDS_OUT0_LN2_M	>	LVDS	SoC VideoOut LVDS ch0 Data2-	SoC VideoOut LVDS ch0 Data2-
39	LVDS_OUT0_LN3_P	>	LVDS	SoC VideoOut LVDS ch0 Data3+	SoC VideoOut LVDS ch0 Data3+
40	LVDS_OUT0_LN3_M	>	LVDS	SoC VideoOut LVDS ch0 Data3-	SoC VideoOut LVDS ch0 Data3-
43	LVDS_IN0_CLK_P *2	<	LVDS	SoC VideoIn LVDS ch0 Clock+	SoC VideoIn LVDS ch0 Clock+
44	LVDS_IN0_CLK_M *2	<	LVDS	SoC VideoIn LVDS ch0 Clock-	SoC VideoIn LVDS ch0 Clock-
45	LVDS_IN0_LN0_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data0+	SoC VideoIn LVDS ch0 Data0+
46	LVDS_IN0_LN0_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data0-	SoC VideoIn LVDS ch0 Data0-
47	LVDS_IN0_LN1_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data1+	SoC VideoIn LVDS ch0 Data1+
48	LVDS_IN0_LN1_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data1-	SoC VideoIn LVDS ch0 Data1-
49	LVDS_IN0_LN2_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data2+	SoC VideoIn LVDS ch0 Data2+
50	LVDS_IN0_LN2_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data2-	SoC VideoIn LVDS ch0 Data2-
51	LVDS_IN0_LN3_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data3+	SoC VideoIn LVDS ch0 Data3+
52	LVDS_IN0_LN3_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data3-	SoC VideoIn LVDS ch0 Data3-
7	GPIO_VOUT0_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Enable
8	GPIO_VOUT0_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Detect/Interrupt
9	GPIO_VOUT0_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Reset
10	GPIO_VOUT0_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO
3	GPIO_VIN2_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
4	GPIO_VIN2_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
5	GPIO_VIN2_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
6	GPIO_VIN2_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO

Pin	Signal Name	Direction Control - VOUT0	Voltage	Connection of the control board	Description Example of use
16	SERIF_VOUT0_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
17	SERIF_VOUT0_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
18	SERIF_VOUT0_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
19	SERIF_VOUT0_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
12	SERIF_VIN0_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
13	SERIF_VIN0_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
14	SERIF_VIN0_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
15	SERIF_VIN0_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
21	I2S_VOUT0_DATA	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2S Data
22	I2S_VOUT0_LRCLK	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2S LR Clock
23	I2S_VOUT0_BCLK	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2S Bit Clock
55	I2S_VOUT0_MCLK *2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2S Master Clock
1	BOARD_VOUT0_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_0" pin, Pull-up	VideoOut0 Board ID bit0
2	BOARD_VOUT0_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_1" pin, Pull-up	VideoOut0 Board ID bit1
25	BOARD_VOUT0_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_2" pin, Pull-up	VideoOut0 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT0	Voltage	Connection of the control board	Description Example of use
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board

*2: The signal is connected to VideoIn0 as well. If used on VideoIn0 Board, output conflict should be avoided

1.3.3. VideoOut1 Board Interface (R-Car H3 Reference Hardware)

Figure 5 shows a schematic illustrating simplified connections between Control Board and VideoOut1 Board in R-Car H3 Reference Hardware. Connector (VOUT1 CN) pin assignments and connected terminals are listed on Table 4.

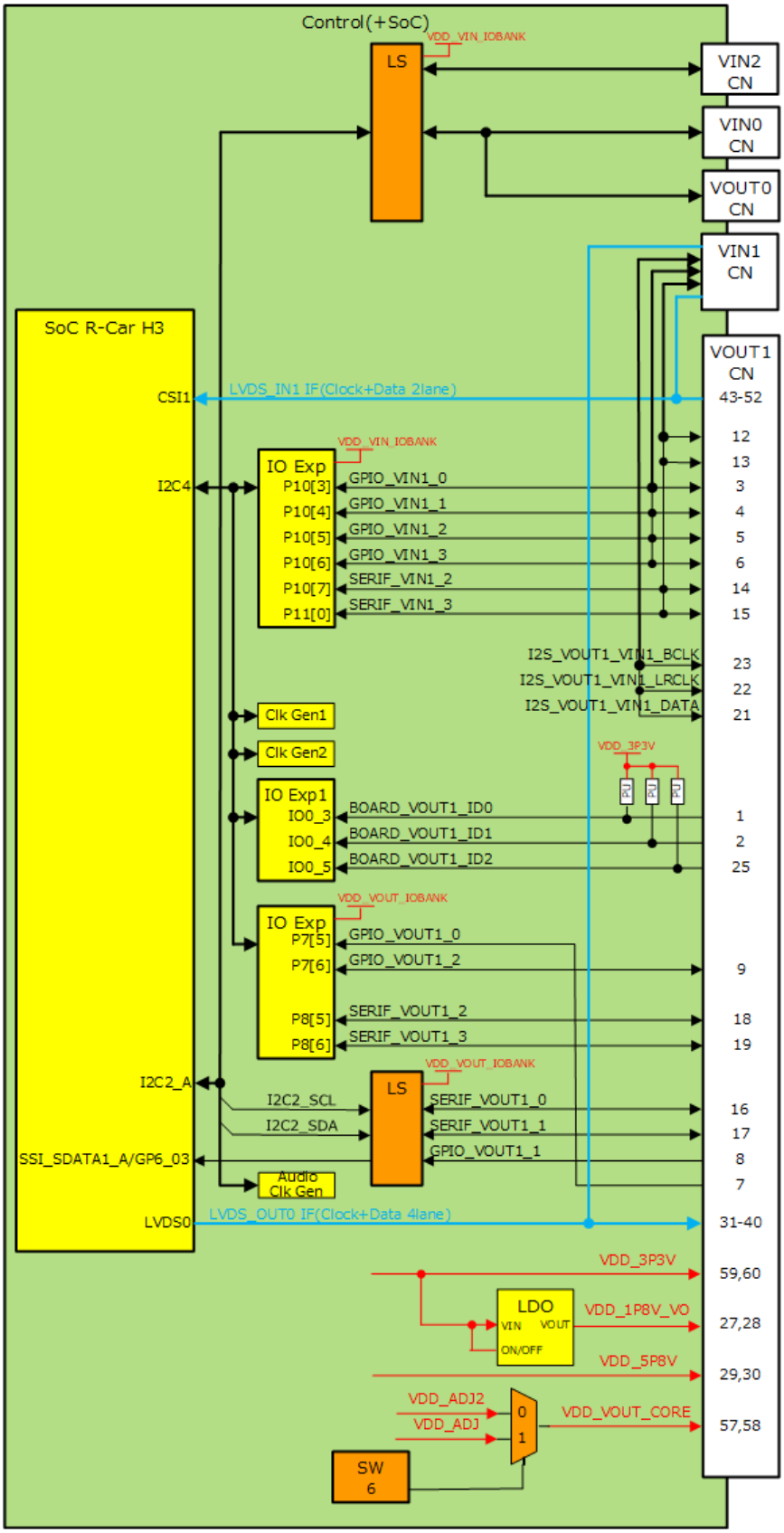


Figure 5 Connectivity between VideoOut1 Board and Control Board (R-Car H3 Reference Hardware)

Table 4 Connector (VOUT1 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - VOUT1	Voltage	Connection of the control board	Description
31	LVDS_OUT1_CLK_P	>	LVDS	R-Car H3 "LVDS0_CLK_P" pin	No used
32	LVDS_OUT1_CLK_M	>	LVDS	R-Car H3 "LVDS0_CLK_N" pin	No used
33	LVDS_OUT1_LN0_P	>	LVDS	R-Car H3 "LVDS0_CH0_P" pin	No used
34	LVDS_OUT1_LN0_M	>	LVDS	R-Car H3 "LVDS0_CH0_N" pin	No used
35	LVDS_OUT1_LN1_P	>	LVDS	R-Car H3 "LVDS0_CH1_P" pin	No used
36	LVDS_OUT1_LN1_M	>	LVDS	R-Car H3 "LVDS0_CH1_N" pin	No used
37	LVDS_OUT1_LN2_P	>	LVDS	R-Car H3 "LVDS0_CH2_P" pin	No used
38	LVDS_OUT1_LN2_M	>	LVDS	R-Car H3 "LVDS0_CH2_N" pin	No used
39	LVDS_OUT1_LN3_P	>	LVDS	R-Car H3 "LVDS0_CH3_P" pin	No used
40	LVDS_OUT1_LN3_M	>	LVDS	R-Car H3 "LVDS0_CH3_N" pin	No used
43	LVDS_IN1_CLK_P	<	LVDS	R-Car H3 "CSI1_CLKP" pin	No used
44	LVDS_IN1_CLK_M	<	LVDS	R-Car H3 "CSI1_CLKN" pin	No used
45	LVDS_IN1_LN0_P	<	LVDS	R-Car H3 "CSI1_DATAP0" pin	No used
46	LVDS_IN1_LN0_M	<	LVDS	R-Car H3 "CSI1_DATAN0" pin	No used
47	LVDS_IN1_LN1_P	<	LVDS	R-Car H3 "CSI1_DATAP1" pin	No used
48	LVDS_IN1_LN1_M	<	LVDS	R-Car H3 "CSI1_DATAN1" pin	No used
49	LVDS_IN1_LN2_P	-	-	NC	-
50	LVDS_IN1_LN2_M	-	-	NC	-
51	LVDS_IN1_LN3_P	-	-	NC	-
52	LVDS_IN1_LN3_M	-	-	NC	-
7	GPIO_VOUT1_0	<>	3.3[V] *2	IO Expander-7 bit5	No used
8	GPIO_VOUT1_1	<	3.3[V] *2	R-Car H3 "SSI_SDATA1_A/GP6_03" pin	No used
9	GPIO_VOUT1_2	<>	3.3[V] *2	IO Expander-7 bit6	No used
10	GPIO_VOUT1_3	-	-	NC	-
3	GPIO_VIN1_0	<>	3.3[V] *3	IO Expander-10 bit3	No used
4	GPIO_VIN1_1	<>	3.3[V] *3	IO Expander-10 bit4	No used
5	GPIO_VIN1_2	<>	3.3[V] *3	IO Expander-10 bit5	No used
6	GPIO_VIN1_3	<>	3.3[V] *3	IO Expander-10 bit6	No used

Pin	Signal Name	Direction Control - VOUT1	Voltage	Connection of the control board	Description
16	SERIF_VOUT1_0	<>	3.3[V] *2	R-Car H3 "RTS0#/SCL2_A" pin	No used
17	SERIF_VOUT1_1	<>	3.3[V] *2	R-Car H3 "SCK0/SDA2_A" pin	No used
18	SERIF_VOUT1_2	<>	3.3[V] *2	IO Expander-10 bit7	No used
19	SERIF_VOUT1_3	<>	3.3[V] *2	IO Expander-11 bit0	No used
12	SERIF_VIN1_0	-	-	NC	-
13	SERIF_VIN1_1	-	-	NC	-
14	SERIF_VIN1_2	<>	3.3[V] *3	IO Expander-10 bit7	No used
15	SERIF_VIN1_3	<>	3.3[V] *3	IO Expander-11 bit0	No used
21	I2S_VOUT1_VIN1_DATA	-	-	No used	-
22	I2S_VOUT1_VIN1_LRCLK	-	-	No used	-
23	I2S_VOUT1_VIN1_BCLK	-	-	No used	-
55	-	-	-	NC	-
1	BOARD_VOUT1_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_3" pin, Pull-up	VideoOut1 Board ID bit0
2	BOARD_VOUT1_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_4" pin, Pull-up	VideoOut1 Board ID bit1
25	BOARD_VOUT1_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_5" pin, Pull-up	VideoOut1 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT1	Voltage	Connection of the control board	Description
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VOUT IO voltage) on Control Board
*3: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control Board

1.3.4. VideoOut1 Board Interface (Standard Reference Hardware)

Table 7Figure 6 shows a schematic of Control Board with VOUT1 CN that connects to VideoOut1 Board in Standard Reference Hardware. Pin assignments of the connector (VOUT1 CN) and connected terminals are listed on Table 5. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

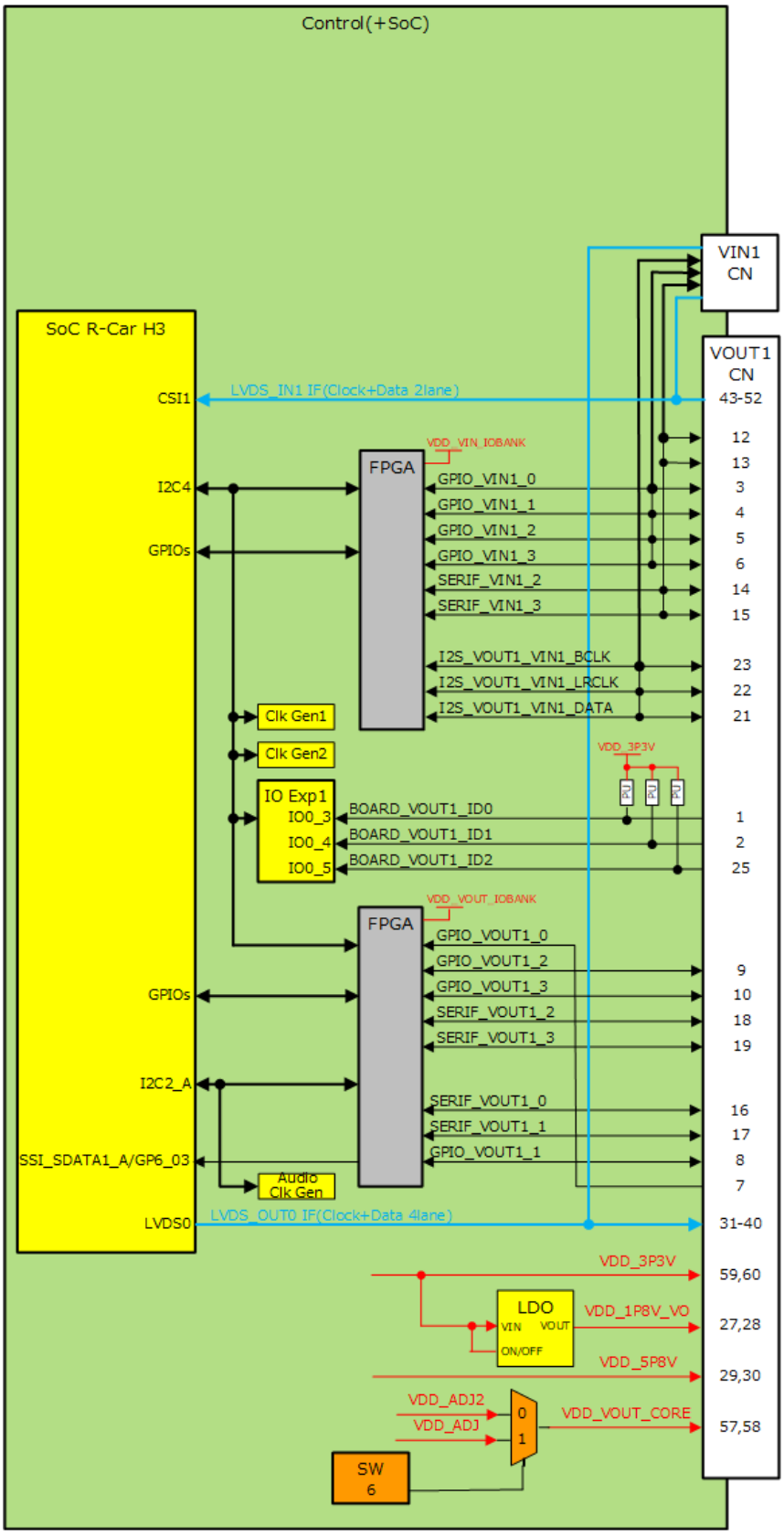


Figure 6 Connectivity between VideoOut1 Board and Control Board (Standard Reference Hardware)

Table 5 Connector (VOUT1 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control – VOUT1	Voltage	Connection of the control board	Description Example of use
31	LVDS_OUT1_CLK_P	>	LVDS	SoC VideoOut LVDS ch0 Clock+	SoC VideoOut LVDS ch0 Clock+
32	LVDS_OUT1_CLK_M	>	LVDS	SoC VideoOut LVDS ch0 Clock-	SoC VideoOut LVDS ch0 Clock-
33	LVDS_OUT1_LN0_P	>	LVDS	SoC VideoOut LVDS ch0 Data0+	SoC VideoOut LVDS ch0 Data0+
34	LVDS_OUT1_LN0_M	>	LVDS	SoC VideoOut LVDS ch0 Data0-	SoC VideoOut LVDS ch0 Data0-
35	LVDS_OUT1_LN1_P	>	LVDS	SoC VideoOut LVDS ch0 Data1+	SoC VideoOut LVDS ch0 Data1+
36	LVDS_OUT1_LN1_M	>	LVDS	SoC VideoOut LVDS ch0 Data1-	SoC VideoOut LVDS ch0 Data1-
37	LVDS_OUT1_LN2_P	>	LVDS	SoC VideoOut LVDS ch0 Data2+	SoC VideoOut LVDS ch0 Data2+
38	LVDS_OUT1_LN2_M	>	LVDS	SoC VideoOut LVDS ch0 Data2-	SoC VideoOut LVDS ch0 Data2-
39	LVDS_OUT1_LN3_P	>	LVDS	SoC VideoOut LVDS ch0 Data3+	SoC VideoOut LVDS ch0 Data3+
40	LVDS_OUT1_LN3_M	>	LVDS	SoC VideoOut LVDS ch0 Data3-	SoC VideoOut LVDS ch0 Data3-
43	LVDS_IN1_CLK_P *2	<	LVDS	SoC VideoIn LVDS ch0 Clock+	SoC VideoIn LVDS ch0 Clock+
44	LVDS_IN1_CLK_M *2	<	LVDS	SoC VideoIn LVDS ch0 Clock-	SoC VideoIn LVDS ch0 Clock-
45	LVDS_IN1_LN0_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data0+	SoC VideoIn LVDS ch0 Data0+
46	LVDS_IN1_LN0_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data0-	SoC VideoIn LVDS ch0 Data0-
47	LVDS_IN1_LN1_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data1+	SoC VideoIn LVDS ch0 Data1+
48	LVDS_IN1_LN1_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data1-	SoC VideoIn LVDS ch0 Data1-
49	LVDS_IN1_LN2_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data2+	SoC VideoIn LVDS ch0 Data2+
50	LVDS_IN1_LN2_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data2-	SoC VideoIn LVDS ch0 Data2-
51	LVDS_IN1_LN3_P *2	<	LVDS	SoC VideoIn LVDS ch0 Data3+	SoC VideoIn LVDS ch0 Data3+
52	LVDS_IN1_LN3_M *2	<	LVDS	SoC VideoIn LVDS ch0 Data3-	SoC VideoIn LVDS ch0 Data3-
7	GPIO_VOUT1_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Enable
8	GPIO_VOUT1_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Detect/Interrupt
9	GPIO_VOUT1_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Reset
10	GPIO_VOUT1_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO
3	GPIO_VIN1_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
4	GPIO_VIN1_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
5	GPIO_VIN1_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
6	GPIO_VIN1_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO

Pin	Signal Name	Direction Control – VOUT1	Voltage	Connection of the control board	Description Example of use
16	SERIF_VOUT1_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
17	SERIF_VOUT1_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
18	SERIF_VOUT1_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
19	SERIF_VOUT1_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
12	SERIF_VIN1_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
13	SERIF_VIN1_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
14	SERIF_VIN1_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
15	SERIF_VIN1_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO
21	I2S_VOUT1_VIN1_DATA *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Data
22	I2S_VOUT1_VIN1_LRCLK *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S LR Clock
23	I2S_VOUT1_VIN1_BCLK *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Bit Clock
55	-	-	-	NC	-
1	BOARD_VOUT1_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_3" pin, Pull-up	VideoOut1 Board ID bit0
2	BOARD_VOUT1_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_4" pin, Pull-up	VideoOut1 Board ID bit1
25	BOARD_VOUT1_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_5" pin, Pull-up	VideoOut1 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control – VOUT1	Voltage	Connection of the control board	Description Example of use
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board

*2: The signal is connected to VideoIn1 as well. If used on VideoIn1 Board, output conflict should be avoided.

1.3.5. VideoOut2 Board Interface (R-Car H3 Reference Hardware)

Figure 7 shows a schematic illustrating simplified connections between Control Board and VideoOut2 Board in R-Car H3 Reference Hardware. Connector (VOUT2 CN) pin assignments and connected terminals are listed on Table 6.

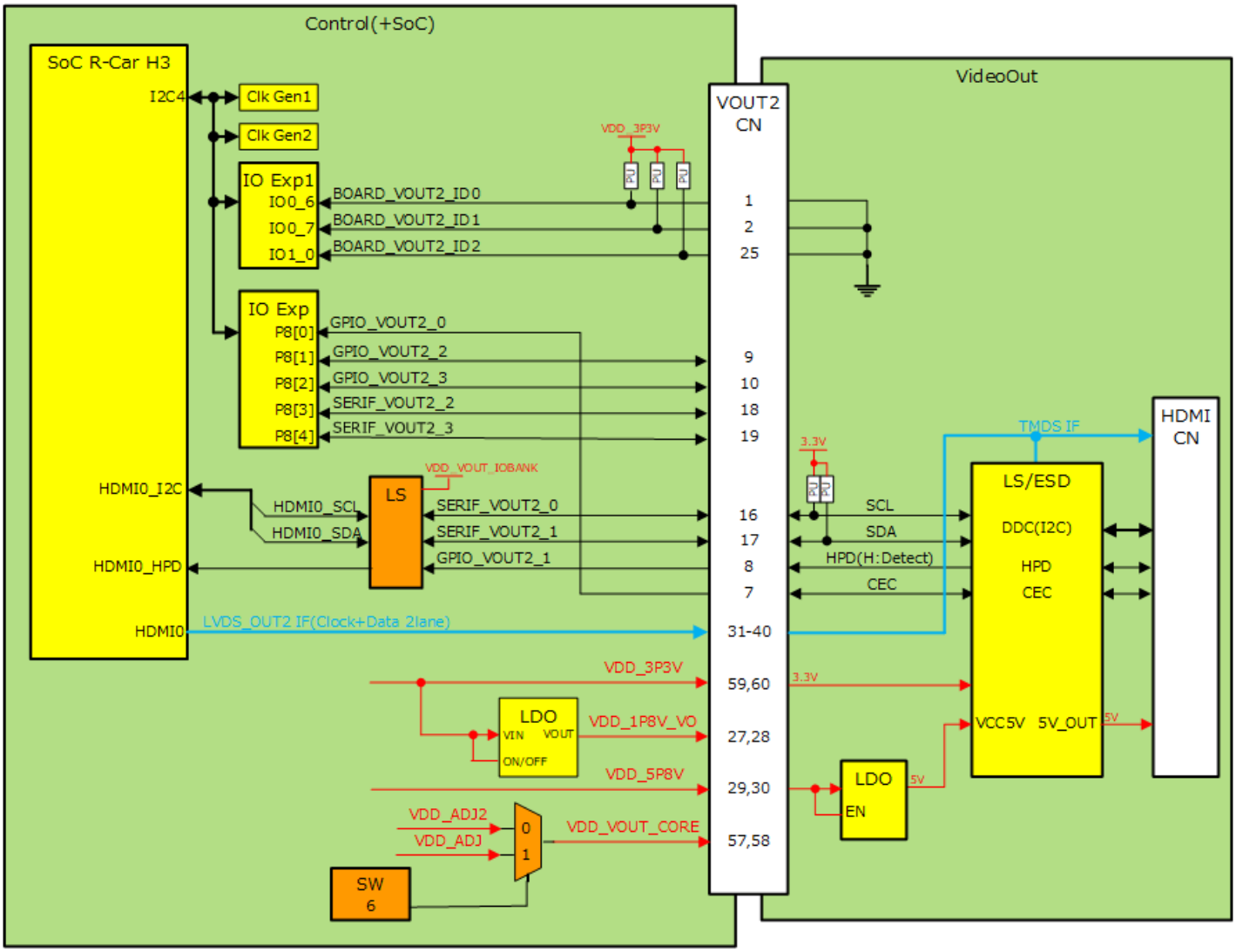


Figure 7 Connectivity between VideoOut2 Board and Control Board (R-Car H3 Reference Hardware)

Table 6 Connector (VOUT2 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description
31	LVDS_OUT2_CLK_P	>	LVDS	R-Car H3 "HDMI0_TMDSCLKP" pin	HDMI ch0 TMDS Clock+
32	LVDS_OUT2_CLK_M	>	LVDS	R-Car H3 "HDMI0_TMDSCLKN" pin	HDMI ch0 TMDS Clock-
33	LVDS_OUT2_LN0_P	>	LVDS	R-Car H3 "HDMI0_TMDSDATAP0" pin	HDMI ch0 TMDS Data0+
34	LVDS_OUT2_LN0_M	>	LVDS	R-Car H3 "HDMI0_TMDSDATAN0" pin	HDMI ch0 TMDS Data0-
35	LVDS_OUT2_LN1_P	>	LVDS	R-Car H3 "HDMI0_TMDSDATAP1" pin	HDMI ch0 TMDS Data1+
36	LVDS_OUT2_LN1_M	>	LVDS	R-Car H3 "HDMI0_TMDSDATAN1" pin	HDMI ch0 TMDS Data1-
37	LVDS_OUT2_LN2_P	>	LVDS	R-Car H3 "HDMI0_TMDSDATAP2" pin	HDMI ch0 TMDS Data2+
38	LVDS_OUT2_LN2_M	>	LVDS	R-Car H3 "HDMI0_TMDSDATAN2" pin	HDMI ch0 TMDS Data2-
39	LVDS_OUT2_LN3_P	-	-	NC	-
40	LVDS_OUT2_LN3_M	-	-	NC	-
43	-	-	-	NC	-
44	-	-	-	NC	-
45	-	-	-	NC	-
46	-	-	-	NC	-
47	-	-	-	NC	-
48	-	-	-	NC	-
49	-	-	-	NC	-
50	-	-	-	NC	-
51	-	-	-	NC	-
52	-	-	-	NC	-
7	GPIO_VOUT2_0	<>	3.3[V] *2	IO Expander-8 bit0	No used
8	GPIO_VOUT2_1	<	3.3[V] *2	R-Car H3 "HDMI0_HPD" pin	HDMI ch1 Hot plug detect
9	GPIO_VOUT2_2	<>	3.3[V] *2	IO Expander-8 bit1	No used
10	GPIO_VOUT2_3	<>	3.3[V] *2	IO Expander-8 bit2	No used
3	-	-	-	NC	-
4	-	-	-	NC	-
5	-	-	-	NC	-
6	-	-	-	NC	-

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description
16	SERIF_VOUT2_0	<>	3.3[V] *2	R-Car H3 "HDMI0_SCL" pin	HDMI ch0 DDC SCL
17	SERIF_VOUT2_1	<>	3.3[V] *2	R-Car H3 "HDMI0_SDA" pin	HDMI ch0 DDC SDA
18	SERIF_VOUT2_2	<>	3.3[V] *2	IO Expander-8 bit3	No used
19	SERIF_VOUT2_3	<>	3.3[V] *2	IO Expander-8 bit4	No used
12	-	-	-	NC	-
13	-	-	-	NC	-
14	-	-	-	NC	-
15	-	-	-	NC	-
21	-	-	-	NC	-
22	-	-	-	NC	-
23	-	-	-	NC	-
55	-	-	-	NC	-
1	BOARD_VOUT2_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_6" pin, Pull-up	VideoOut2 Board ID bit0
2	BOARD_VOUT2_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_7" pin, Pull-up	VideoOut2 Board ID bit1
25	BOARD_VOUT2_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_8" pin, Pull-up	VideoOut2 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VOUT IO voltage) on Control Board

1.3.6. VideoOut2 Board Interface (Standard Reference Hardware)

Figure 8 shows a schematic of Control Board with VOUT2 CN that connects to VideoOut2 Board in Standard Reference Hardware. Pin assignments of the connector (VOUT2 CN) and connected terminals are listed on Table 7. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

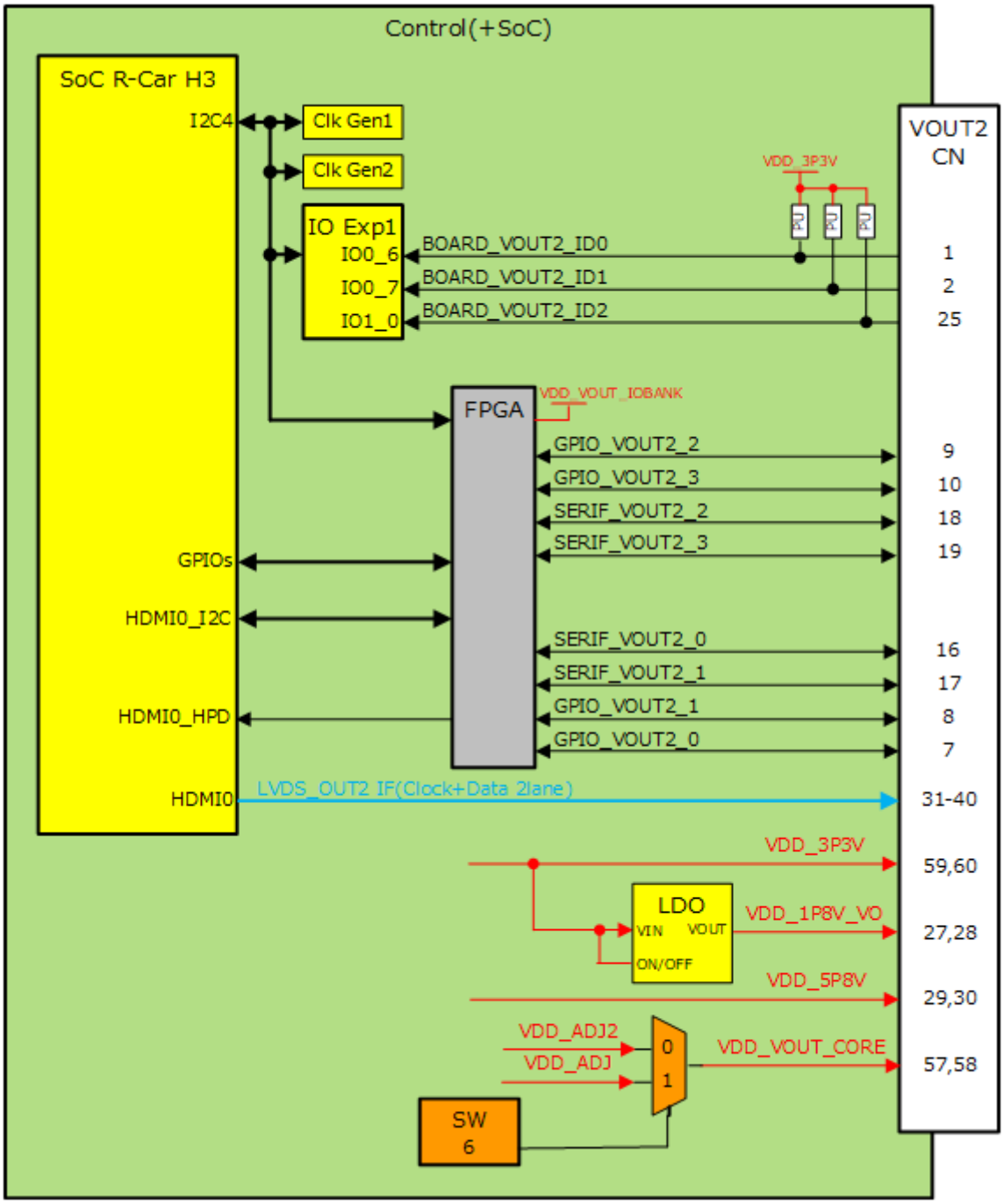


Figure 8 Connectivity between VideoOut2 Board and Control Board (Standard Reference Hardware)

Table 7 Connector (VOUT2 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description Example of use
31	LVDS_OUT2_CLK_P	>	LVDS	SoC VideoOut LVDS ch2 Clock+	SoC VideoOut LVDS ch2 Clock+
32	LVDS_OUT2_CLK_M	>	LVDS	SoC VideoOut LVDS ch2 Clock-	SoC VideoOut LVDS ch2 Clock-
33	LVDS_OUT2_LN0_P	>	LVDS	SoC VideoOut LVDS ch2 Data0+	SoC VideoOut LVDS ch2 Data0+
34	LVDS_OUT2_LN0_M	>	LVDS	SoC VideoOut LVDS ch2 Data0-	SoC VideoOut LVDS ch2 Data0-
35	LVDS_OUT2_LN1_P	>	LVDS	SoC VideoOut LVDS ch2 Data1+	SoC VideoOut LVDS ch2 Data1+
36	LVDS_OUT2_LN1_M	>	LVDS	SoC VideoOut LVDS ch2 Data1-	SoC VideoOut LVDS ch2 Data1-
37	LVDS_OUT2_LN2_P	>	LVDS	SoC VideoOut LVDS ch2 Data2+	SoC VideoOut LVDS ch2 Data2+
38	LVDS_OUT2_LN2_M	>	LVDS	SoC VideoOut LVDS ch2 Data2-	SoC VideoOut LVDS ch2 Data2-
39	LVDS_OUT2_LN3_P	>	LVDS	SoC VideoOut LVDS ch2 Data3+	SoC VideoOut LVDS ch2 Data3+
40	LVDS_OUT2_LN3_M	>	LVDS	SoC VideoOut LVDS ch2 Data3-	SoC VideoOut LVDS ch2 Data3-
43	-	-	-	NC	-
44	-	-	-	NC	-
45	-	-	-	NC	-
46	-	-	-	NC	-
47	-	-	-	NC	-
48	-	-	-	NC	-
49	-	-	-	NC	-
50	-	-	-	NC	-
51	-	-	-	NC	-
52	-	-	-	NC	-
7	GPIO_VOUT2_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Enable
8	GPIO_VOUT2_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Detect/Interrupt
9	GPIO_VOUT2_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. Reset
10	GPIO_VOUT2_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO
3	-	-	-	NC	-
4	-	-	-	NC	-
5	-	-	-	NC	-
6	-	-	-	NC	-

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description Example of use
16	SERIF_VOUT2_0	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
17	SERIF_VOUT2_1	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
18	SERIF_VOUT2_2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
19	SERIF_VOUT2_3	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
12	-	-	-	NC	-
13	-	-	-	NC	-
14	-	-	-	NC	-
15	-	-	-	NC	-
21	-	-	-	NC	-
22	-	-	-	NC	-
23	-	-	-	NC	-
55	-	-	-	NC	-
1	BOARD_VOUT2_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_6" pin, Pull-up	VideoOut2 Board ID bit0
2	BOARD_VOUT2_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_7" pin, Pull-up	VideoOut2 Board ID bit1
25	BOARD_VOUT2_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO0_8" pin, Pull-up	VideoOut2 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT2	Voltage	Connection of the control board	Description Example of use
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board

1.3.7. VideoOut3 Board Interface (R-Car H3 Reference Hardware)

Figure 9 shows a schematic illustrating simplified connections between Control Board and VideoOut3 Board in R-Car H3 Reference Hardware. Connector (VOUT3 CN) pin assignments and connected terminals are listed on Table 8.

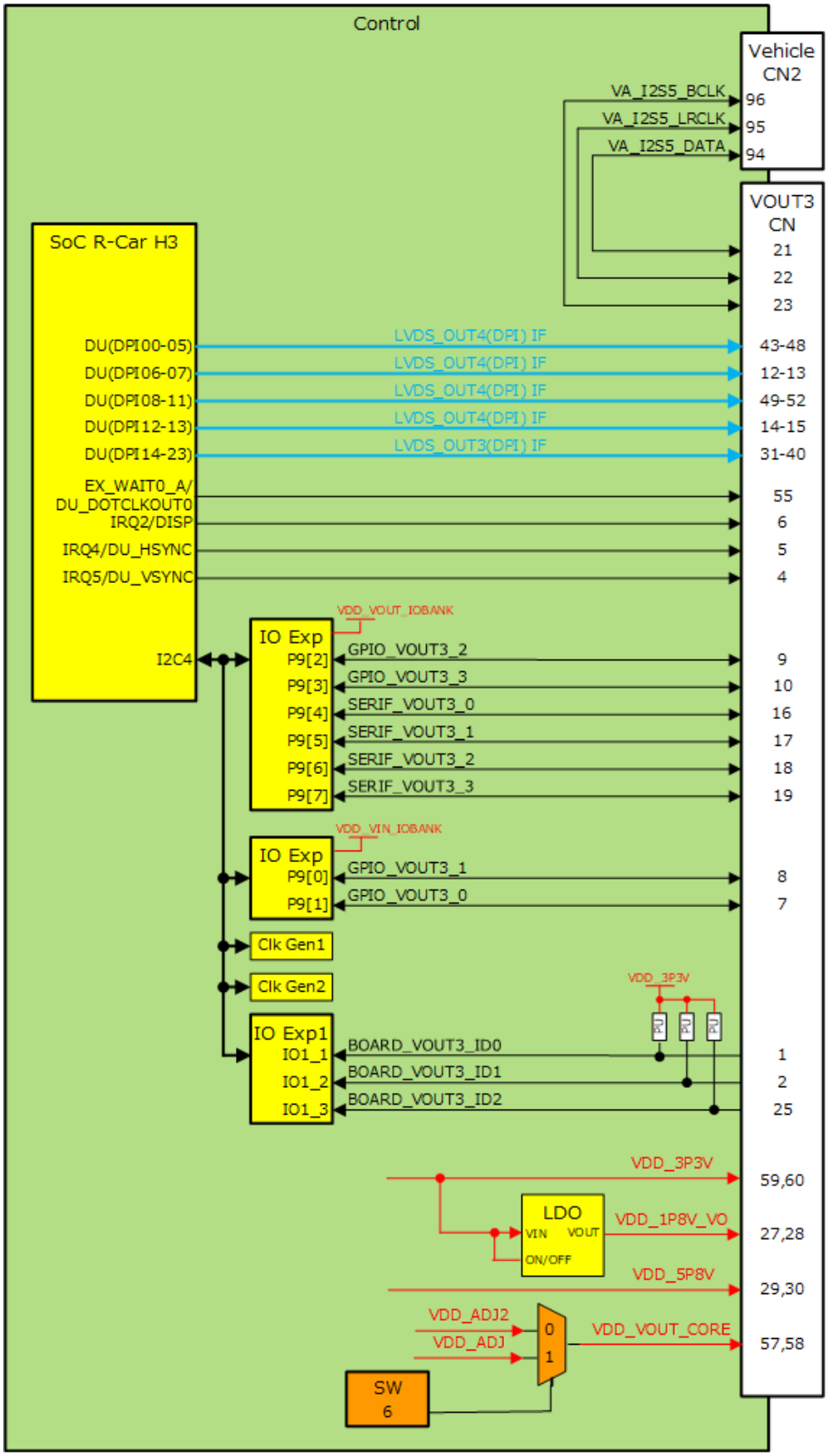


Figure 9 Connectivity between VideoOut3 Board and Control Board (R-Car H3 Reference Hardware)

Table 8 Connector (VOUT3 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description
31	LVDS_OUT3_CLK_P/DPI14	>	3.3[V]	R-Car H3 "A14/DU_DG6" pin	No used
32	LVDS_OUT3_CLK_M/DPI15	>	3.3[V]	R-Car H3 "A15/DU_DG7" pin	No used
33	LVDS_OUT3_LN0_P/DPI16	>	3.3[V]	R-Car H3 "D8/DU_DR0" pin	No used
34	LVDS_OUT3_LN0_M/DPI17	>	3.3[V]	R-Car H3 "D9/DU_DR1" pin	No used
35	LVDS_OUT3_LN1_P/DPI18	>	3.3[V]	R-Car H3 "D10/DU_DR2" pin	No used
36	LVDS_OUT3_LN1_M/DPI19	>	3.3[V]	R-Car H3 "D11/DU_DR3" pin	No used
37	LVDS_OUT3_LN2_P/DPI20	>	3.3[V]	R-Car H3 "D12/DU_DR4" pin	No used
38	LVDS_OUT3_LN2_M/DPI21	>	3.3[V]	R-Car H3 "D13/DU_DR5" pin	No used
39	LVDS_OUT3_LN3_P/DPI22	>	3.3[V]	R-Car H3 "D14/DU_DR6" pin	No used
40	LVDS_OUT3_LN3_M/DPI23	>	3.3[V]	R-Car H3 "D15/DU_DR7" pin	No used
43	LVDS_OUT4_LN0_M/DPI00	>	3.3[V]	R-Car H3 "A0/DU_DB0" pin	No used
44	LVDS_OUT4_LN0_P/DPI01	>	3.3[V]	R-Car H3 "A1/DU_DB1" pin	No used
45	LVDS_OUT4_LN1_M/DPI02	>	3.3[V]	R-Car H3 "A2/DU_DB2" pin	No used
46	LVDS_OUT4_LN1_P/DPI03	>	3.3[V]	R-Car H3 "A3/DU_DB3" pin	No used
47	LVDS_OUT4_LN2_M/DPI04	>	3.3[V]	R-Car H3 "A4/DU_DB4" pin	No used
48	LVDS_OUT4_LN2_P/DPI05	>	3.3[V]	R-Car H3 "A5/DU_DB5" pin	No used
49	LVDS_OUT4_LN4_M/DPI08	>	3.3[V]	R-Car H3 "A16/DU_DG0" pin	No used
50	LVDS_OUT4_LN4_P/DPI09	>	3.3[V]	R-Car H3 "A17/DU_DG1" pin	No used
51	LVDS_OUT4_LN5_M/DPI10	>	3.3[V]	R-Car H3 "A18/DU_DG2" pin	No used
52	LVDS_OUT4_LN5_P/DPI11	>	3.3[V]	R-Car H3 "A19/DU_DG3" pin	No used
7	GPIO_VOUT3_0	<>	3.3[V] *3	IO Expander-9 bit1	No used
8	GPIO_VOUT3_1	<>	3.3[V] *3	IO Expander-9 bit0	No used
9	GPIO_VOUT3_2	<>	3.3[V] *2	IO Expander-9 bit2	No used
10	GPIO_VOUT3_3	<>	3.3[V] *2	IO Expander-9 bit3	No used
3	DPI_DCLK_IN	-	-	NC	-
4	DPI_VSYNC	>	3.3[V]	R-Car H3 "IRQ5/DU_VSYNC" pin	No used
5	DPI_HSYNC	>	3.3[V]	R-Car H3 "IRQ4/DU_HSYNC" pin	No used

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description
6	DPI_ETC	>	3.3[V]	R-Car H3 "IRQ2/DU_ODDF/DISP" pin	No used
16	SERIF_VOUT3_0	<>	3.3[V] *2	IO Expander-9 bit4	No used
17	SERIF_VOUT3_1	<>	3.3[V] *2	IO Expander-9 bit5	No used
18	SERIF_VOUT3_2	<>	3.3[V] *2	IO Expander-9 bit6	No used
19	SERIF_VOUT3_3	<>	3.3[V] *2	IO Expander-9 bit7	No used
12	LVDS_OUT4_LN3_M/DPI06	>	3.3[V]	R-Car H3 "A6/DU_DB6" pin	No used
13	LVDS_OUT4_LN3_P/DPI07	>	3.3[V]	R-Car H3 "A7/DU_DB7" pin	No used
14	LVDS_OUT4_LN6_M/DPI12	>	3.3[V]	R-Car H3 "A12/DU_DG4" pin	No used
15	LVDS_OUT4_LN6_P/DPI13	>	3.3[V]	R-Car H3 "A13/DU_DG5" pin	No used
21	VA_I2S5_DATA	<>	-	NC	-
22	VA_I2S5_LRCLK	<>	-	NC	-
23	VA_I2S5_BCLK	<>	-	NC	-
55	DPI_DCLK_OUT	>	3.3[V]	R-Car H3 "EX_WAIT0_A/DU_DOTCLKOUT0" pin	No used
1	BOARD_VOUT3_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_1" pin, Pull-up	VideoOut3 Board ID bit0
2	BOARD_VOUT3_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_2" pin, Pull-up	VideoOut3 Board ID bit1
25	BOARD_VOUT3_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_3" pin, Pull-up	VideoOut3 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VOUT IO voltage) on Control Board
*3: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control Board

1.3.8. VideoOut3 Board Interface (Standard Reference Hardware)

Figure 10 shows a schematic of Control Board with VOUT3 CN that connects to VideoOut3 Board in Standard Reference Hardware. Pin assignments of the connector (VOUT3 CN) and connected terminals are listed on Table 9. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

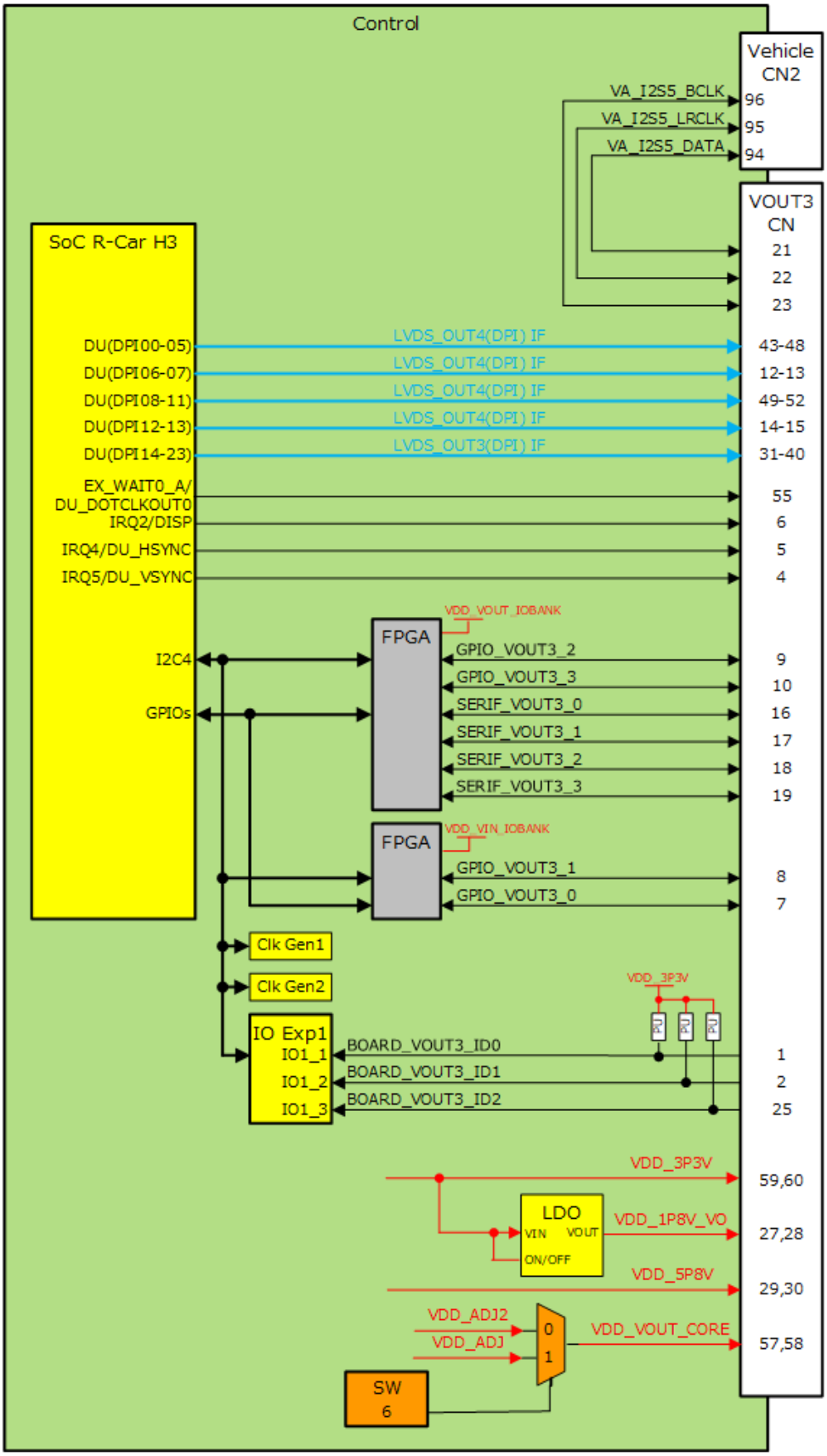


Figure 10 Connectivity between VideoOut3 Board and Control Board (Standard Reference Hardware)

Table 9 Connector (VOUT3 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description Example of use
31	LVDS_OUT3_CLK_P/DPI14	>	VREG_SOC_IO/LVDS	R-Car H3 "A14/DU_DG6" pin	SoC VideoOut DPI bit14/LVDS ch3 Clock+
32	LVDS_OUT3_CLK_M/DPI15	>	VREG_SOC_IO/LVDS	R-Car H3 "A15/DU_DG7" pin	SoC VideoOut DPI bit15/LVDS ch3 Clock-
33	LVDS_OUT3_LN0_P/DPI16	>	VREG_SOC_IO/LVDS	R-Car H3 "D8/DU_DR0" pin	SoC VideoOut DPI bit16/LVDS ch3 Data0+
34	LVDS_OUT3_LN0_M/DPI17	>	VREG_SOC_IO/LVDS	R-Car H3 "D9/DU_DR1" pin	SoC VideoOut DPI bit17/LVDS ch3 Data0-
35	LVDS_OUT3_LN1_P/DPI18	>	VREG_SOC_IO/LVDS	R-Car H3 "D10/DU_DR2" pin	SoC VideoOut DPI bit18/LVDS ch3 Data1+
36	LVDS_OUT3_LN1_M/DPI19	>	VREG_SOC_IO/LVDS	R-Car H3 "D11/DU_DR3" pin	SoC VideoOut DPI bit19/LVDS ch3 Data1-
37	LVDS_OUT3_LN2_P/DPI20	>	VREG_SOC_IO/LVDS	R-Car H3 "D12/DU_DR4" pin	SoC VideoOut DPI bit20/LVDS ch3 Data2+
38	LVDS_OUT3_LN2_M/DPI21	>	VREG_SOC_IO/LVDS	R-Car H3 "D13/DU_DR5" pin	SoC VideoOut DPI bit21/LVDS ch3 Data2-
39	LVDS_OUT3_LN3_P/DPI22	>	VREG_SOC_IO/LVDS	R-Car H3 "D14/DU_DR6" pin	SoC VideoOut DPI bit22/LVDS ch3 Data3+
40	LVDS_OUT3_LN3_M/DPI23	>	VREG_SOC_IO/LVDS	R-Car H3 "D15/DU_DR7" pin	SoC VideoOut DPI bit23/LVDS ch3 Data3-
43	LVDS_OUT4_LN0_M/DPI00	<	VREG_SOC_IO/LVDS	R-Car H3 "A0/DU_DB0" pin	SoC VideoOut DPI bit0/LVDS ch4 Lane0-
44	LVDS_OUT4_LN0_P/DPI01	<	VREG_SOC_IO/LVDS	R-Car H3 "A1/DU_DB1" pin	SoC VideoOut DPI bit1/LVDS ch4 Lane0+
45	LVDS_OUT4_LN1_M/DPI02	<	VREG_SOC_IO/LVDS	R-Car H3 "A2/DU_DB2" pin	SoC VideoOut DPI bit2/LVDS ch4 Lane1-
46	LVDS_OUT4_LN1_P/DPI03	<	VREG_SOC_IO/LVDS	R-Car H3 "A3/DU_DB3" pin	SoC VideoOut DPI bit3/LVDS ch4 Lane1+
47	LVDS_OUT4_LN2_M/DPI04	<	VREG_SOC_IO/LVDS	R-Car H3 "A4/DU_DB4" pin	SoC VideoOut DPI bit4/LVDS ch4 Lane2-
48	LVDS_OUT4_LN2_P/DPI05	<	VREG_SOC_IO/LVDS	R-Car H3 "A5/DU_DB5" pin	SoC VideoOut DPI bit5/LVDS ch4 Lane2+
49	LVDS_OUT4_LN4_M/DPI08	<	VREG_SOC_IO/LVDS	R-Car H3 "A16/DU_DG0" pin	SoC VideoOut DPI bit8/LVDS ch4 Lane4-
50	LVDS_OUT4_LN4_P/DPI09	<	VREG_SOC_IO/LVDS	R-Car H3 "A17/DU_DG1" pin	SoC VideoOut DPI bit9/LVDS ch4 Lane4+
51	LVDS_OUT4_LN5_M/DPI10	<	VREG_SOC_IO/LVDS	R-Car H3 "A18/DU_DG2" pin	SoC VideoOut DPI bit10/LVDS ch4 Lane5-
52	LVDS_OUT4_LN5_P/DPI11	<	VREG_SOC_IO/LVDS	R-Car H3 "A19/DU_DG3" pin	SoC VideoOut DPI bit11/LVDS ch4 Lane5+
7	GPIO_VOUT3_0	<>	VDD_VIN_IOBANK	IO Expander-9 bit1	GPIO, e.g. Enable
8	GPIO_VOUT3_1	<>	VDD_VIN_IOBANK	IO Expander-9 bit0	GPIO, e.g. Detect/Interrupt
9	GPIO_VOUT3_2	<>	VDD_VOUT_IOBANK	IO Expander-9 bit2	GPIO, e.g. Reset
10	GPIO_VOUT3_3	<>	VDD_VOUT_IOBANK	IO Expander-9 bit3	GPIO
3	DPI_DCLK_IN	-	-	NC	-
4	DPI_VSYNC	<>	VREG_SOC_IO	R-Car H3 "IRQ5/DU_VSYNC" pin	SoC VideoOut DPI Vsync
5	DPI_HSYNC	<>	VREG_SOC_IO	R-Car H3 "IRQ4/DU_HSYNC" pin	SoC VideoOut DPI Hsync
6	DPI_ETC	<>	VREG_SOC_IO	R-Car H3 "IRQ2/DU_ODDF/DISP" pin	SoC VideoOut DPI Etc.(Data enable, Field,,,)

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description Example of use
16	SERIF_VOUT3_0	<>	VDD_VOUT_IOBANK	IO Expander-9 bit4	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
17	SERIF_VOUT3_1	<>	VDD_VOUT_IOBANK	IO Expander-9 bit5	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
18	SERIF_VOUT3_2	<>	VDD_VOUT_IOBANK	IO Expander-9 bit6	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
19	SERIF_VOUT3_3	<>	VDD_VOUT_IOBANK	IO Expander-9 bit7	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
12	LVDS_OUT4_LN3_M/DPI06	<>	VREG_SOC_IO/LVDS	R-Car H3 "A6/DU_DB6" pin	SoC VideoOut DPI bit6/LVDS ch4 Lane3-
13	LVDS_OUT4_LN3_P/DPI07	<>	VREG_SOC_IO/LVDS	R-Car H3 "A7/DU_DB7" pin	SoC VideoOut DPI bit7/LVDS ch4 Lane3+
14	LVDS_OUT4_LN6_M/DPI12	<>	VREG_SOC_IO/LVDS	R-Car H3 "A12/DU_DG4" pin	SoC VideoOut DPI bit12/LVDS ch4 Lane6-
15	LVDS_OUT4_LN6_P/DPI13	<>	VREG_SOC_IO/LVDS	R-Car H3 "A13/DU_DG5" pin	SoC VideoOut DPI bit13/LVDS ch4 Lane6+
21	VA_I2S5_DATA	<>	IO_AUDIO	Vehicle CN2 94pin	I2S Data
22	VA_I2S5_LRCLK	<>	IO_AUDIO	Vehicle CN2 95pin	I2S LR Clock
23	VA_I2S5_BCLK	<>	IO_AUDIO	Vehicle CN2 96pin	I2S Bit Clock
55	DPI_DCLK_OUT	>	3.3[V]	R-Car H3 "EX_WAIT0_A/DU_DOTCLKOUT0" pin	SoC VideoOut DPI Dot-clock
1	BOARD_VOUT3_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_1" pin, Pull-up	VideoOut3 Board ID bit0
2	BOARD_VOUT3_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_2" pin, Pull-up	VideoOut3 Board ID bit1
25	BOARD_VOUT3_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_3" pin, Pull-up	VideoOut3 Board ID bit2
27	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
28	VDD_1P8V_VO	>	Power:1.8[V]	1.8[V] output LDO	Power
29	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
30	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
57	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
58	VDD_VOUT_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
59	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
60	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
11	GND	-	GND	GND	GND
20	GND	-	GND	GND	GND
24	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VOUT3	Voltage	Connection of the control board	Description Example of use
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
54	GND	-	GND	GND	GND
26	TP	-	-	NC	-
56	TP	-	-	NC	-

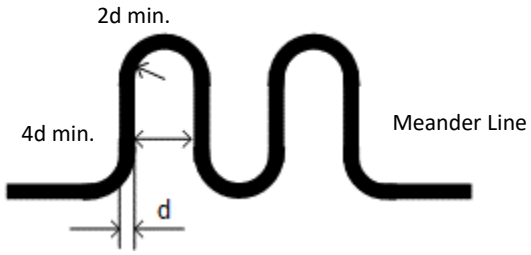
*1: Voltage depends on the power supply switch setting (VOUT Core voltage) on Control Board

1.4. Board Layout Guideline

Due to LVDS lines on Control Board, traces on VideoOut Board need to be designed in accordance with the following restrictions:

Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and –) must be 0.1[mm] maximum.
- Difference between an average length of a clock pair (average of + signal and – signal)/a data signal pair : 0.2[mm] maximum.
- Maximum Trace Length: 60[mm]
- Differential impedance : 100[Ω](100[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace.The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be twice at least the width of the trace. The gap between the meander traces should be at least four times the trace width.



Power Supply

- Comply with power supply requirements (impedance property, etc.) of the device to connect.
  If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[℃] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.

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