Reference Hardware Design Guideline

WLAN Board

Version	Date
1.0	May 25, 2020

Panasonic Corporation

Automotive Company R&D Division

Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

Reference Documents

No.	Document Filename	Ver.	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

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Figures and Tables

1. WLAN Board

WLAN Board is connected to Control Board to communitate data signal with SoCby WLAN and Bluetooth. The interface for WLAN is determined according to SoC design. One PCI-Express x1 channel and one PCI-Express x2 channel are connected to SoC as the interface. Bus such as SDIO can be connected using the same wiring in place of PCI-Express.
UART and PCM are connected for Bluetooth. Antennas are to be built in WLAN board or to be connected separately.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

1.1. Board Outline

The following figure shows WLAN Board dimension. 1.2[mm] is the assumed thickness, but if the change is required, interference with other boards should be considered.
The interface to Control Board is a 60-pin board-to-board connector mounted on the solder side of WLAN Board.

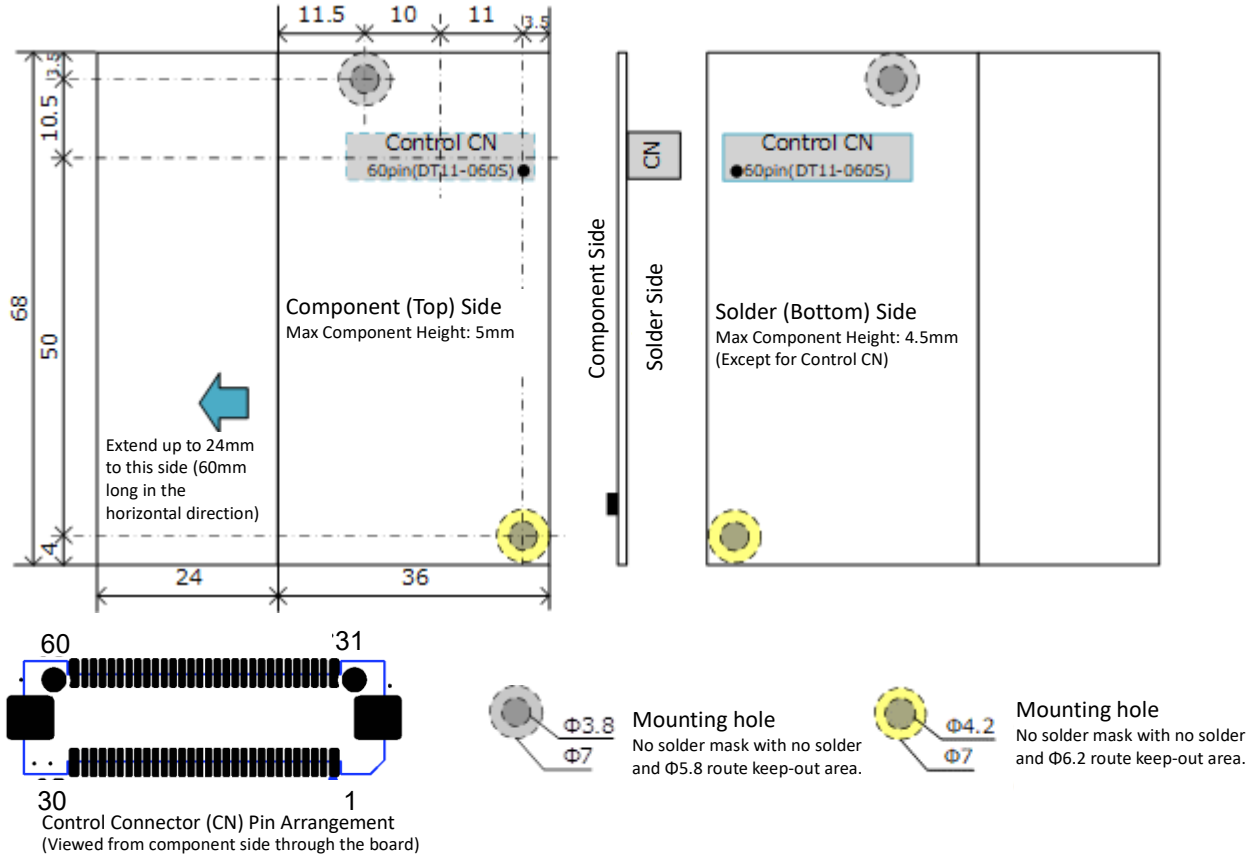


Figure 1 WLAN Board Dimension

1.2. Power Supply

There are four power supply rails that power WLAN Board. The specification of each power supply is shown in Table 1.

Table 1 WLAN Board Power Supply

Power Supply Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
VDD_5P8V		5.87		200	Pin 1, Pin 2 (2 pins)
VPH_PWR_WLAN		3.4 to 5.0		1200	Pin 3, Pin 4, Pin 5 (3 pins) Voltage varies depending on a SoC This voltage is 5V in R-Car H3 Reference Hardware
VDD_WLAN_IO		1.8 or 3.3		100	Pin 31, Pin 32 (2 pins) Voltage varies according to the power supply switch setting on Control Board. 3.3 V is the default setting for R-Car H3 Reference Hardware.
VREG_SOC_IO		SoC dependent		100	Pin 33, Pin 34 (2 pins) This voltage is 3.3V jn R-Car H3 Reference Hardware.

A power circuit can be built on WLAN Board if no power source is available for an intended purpose.

Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, one of the possible solutions is to use another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards). Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins..

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

1.3. Board-to-Board Interface

60-pin board-to-board connectors is used to connect Control Board to WLAN Board. In this document, a receptacle connector (KEL DT01-060S) is on the side of Control Board and a plug connector (KEL DT11-060S-10) is on the side of WLAN board.

These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of ±0.5 [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA]

The voltage for signals interfacing with Control Board should be able to adjust to both 1.8[V] and 3.3[V] as WLAN Board and GNSS Board uses signals of the same terminal voltage. The voltage level should be able to shift using such as a level shifter to make the voltage for signals consistent. When a signal output is on WLAN Board side, and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.

A pull-up or pull-down resistor should be added to WLAN Board for the external resistor required for I2C signal, etc.

When connecting an antenna outside of the board enclosure, the antenna should be connected to Vehicle Board where internally placed WLAN Board is connected via a coaxial cable. A connector used for the coaxial cable is I-PEX's 20279-001E.

1.3.1. WLAN Board Interface (R-Car H3 Reference Hardware)

Figure 2 shows a schematic illustrating simplified connections between Control Board and WLAN Board for R-Car H3 Reference Hardware. Pin assignments of the connector (WLAN CN) and the connected terminals are listed on Table 2.

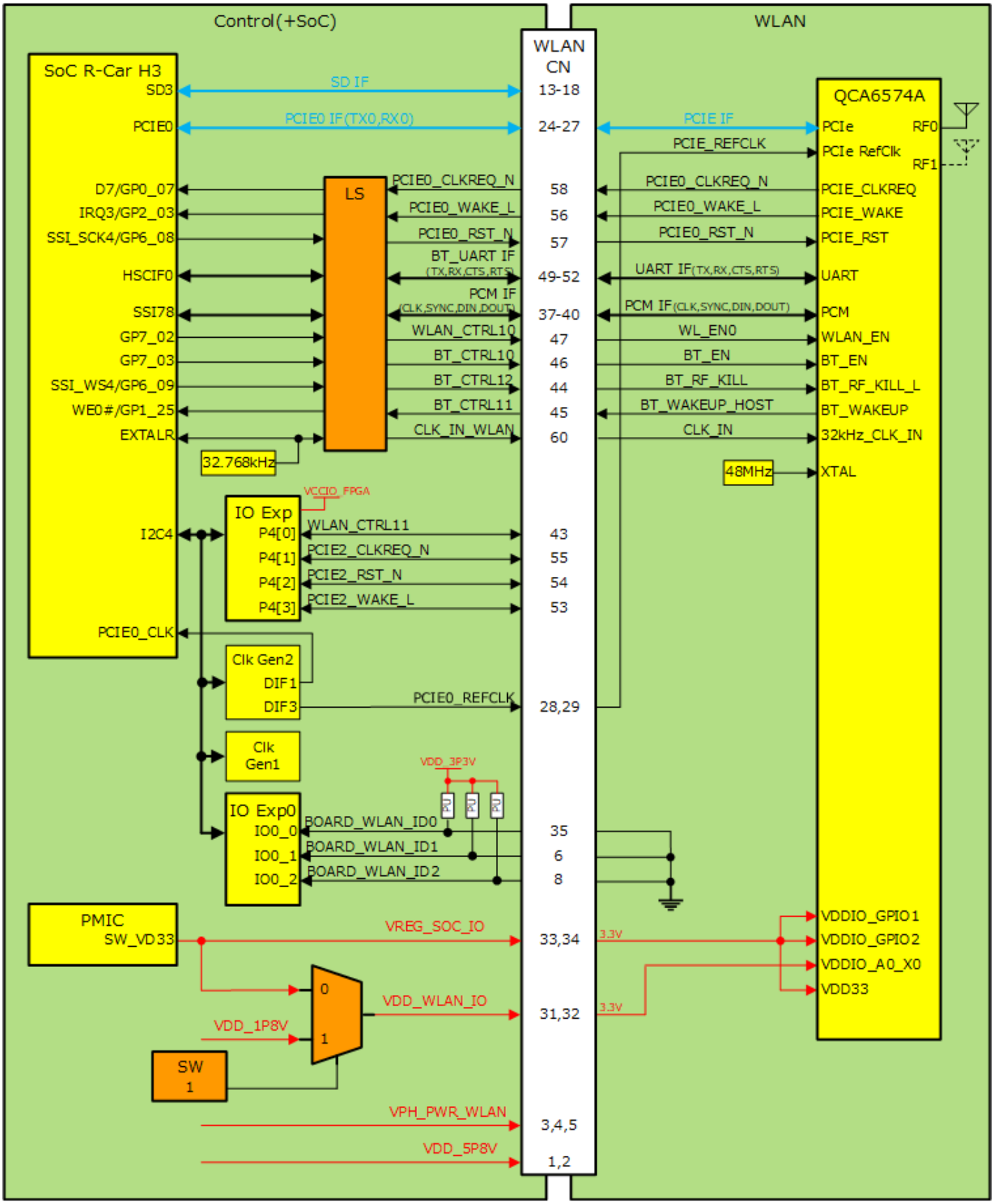


Figure 2 Connectivity between WLAN Board and Control Board (R-Car H3 Reference Hardware)

Table 2 Connector (WLAN CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description
25	PCIE0_TX0_P	>	LVDS	R-Car H3 "PCIE0_TX_P" pin	PCIe ch0 Tx Data+(SoC Tx)
24	PCIE0_TX0_M	>	LVDS	R-Car H3 "PCIE0_TX_M" pin	PCIe ch0 Tx Data-(SoC Tx)
27	PCIE0_RX0_P	<	LVDS	R-Car H3 "PCIE0_RX_P" pin	PCIe ch0 Rx Data+(SoC Rx)
26	PCIE0_RX0_M	<	LVDS	R-Car H3 "PCIE0_RX_M" pin	PCIe ch0 Rx Data-(SoC Rx)
29	PCIE0_REFCLK_P	>	LVDS	Clock generator2(9FGV0841AKILF) "DIF3" pin	PCIe ch0 Reference Clock+
28	PCIE0_REFCLK_M	>	LVDS	Clock generator2(9FGV0841AKILF) "DIF3#" pin	PCIe ch0 Reference Clock-
56	PCIE0_WAKE_L	<	3.3[V]	R-Car H3 "IRQ3/GP2_03" pin	PCIe ch0 Wake Event
57	PCIE0_RST_N	>	3.3[V]	R-Car H3 "SSI_SCK4/GP6_08" pin	PCIe ch0 Reset
58	PCIE0_CLKREQ_N	<	3.3[V]	R-Car H3 "D7/GP0_07" pin	PCIe ch0 Clock Request
15	PCIE2_TX0_P	-	-	NC	-
16	PCIE2_TX0_M	-	-	NC	-
17	PCIE2_RX0_P	-	-	NC	-
18	PCIE2_RX0_M	-	-	NC	-
19	PCIE2_TX1_P	-	-	NC	-
20	PCIE2_TX1_M	-	-	NC	-
21	PCIE2_RX1_P	-	-	NC	-
22	PCIE2_RX1_M	-	-	NC	-
13	PCIE2_REFCLK_P	-	-	NC	-
14	PCIE2_REFCLK_M	-	-	NC	-
53	PCIE2_WAKE_L	<>	3.3[V]	IO Expander-4 bit3	No used
54	PCIE2_RST_N	<>	3.3[V]	IO Expander-4 bit2	No used
55	PCIE2_CLKREQ_N	<>	3.3[V]	IO Expander-4 bit1	No used
60	CLK_IN_WLAN	>	3.3[V]	32.768kHz X'tal	Low-power clock input
47	WLAN_CTRL10	>	3.3[V]	R-Car H3 "GP7_02" pin	WLAN Enable(H:Enable)
43	WLAN_CTRL11	<>	3.3[V]	IO Expander-4 bit0	No used
52	BT_UART_TX	>	3.3[V]	R-Car H3 "HTX0" pin	Bluetooth UART Tx Data(SoC Tx)
51	BT_UART_RX	<	3.3[V]	R-Car H3 "HRX0" pin	Bluetooth UART Rx Data(SoC Rx)
50	BT_UART_CTS	<	3.3[V]	R-Car H3 "HCTS0" pin	Bluetooth UART Control(SoC CTS)

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description
49	BT_UART_RTS	>	3.3[V]	R-Car H3 "HRTS0" pin	Bluetooth UART Control(SoC RTS)
37	PCM_CLK	>	3.3[V]	R-Car H3 "SSI_SCK78" pin	Bluetooth PCM Clock
38	PCM_SYNC	>	3.3[V]	R-Car H3 "SSI_WS78" pin	Bluetooth PCM Sync
39	PCM_DIN	<	3.3[V]	R-Car H3 "SSI_SDATA8" pin	Bluetooth PCM Data In(SoC In)
40	PCM_DOUT	>	3.3[V]	R-Car H3 "SSI_SDATA7" pin	Bluetooth PCM Data Out(SoC Out)
46	BT_CTRL10	>	3.3[V]	R-Car H3 "GP7_03" pin	Bluetooth Enable(H:Enable)
45	BT_CTRL11	<	3.3[V]	R-Car H3 "WE0#/GP1_25" pin	Bluetooth Wakeup host(H:Wakeup)
44	BT_CTRL12	>	3.3[V]	R-Car H3 "SSI_WS4/GP6_09" pin	Bluetooth RF front-end turn-off(L:OFF)
35	BOARD_WLAN_ID0	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_0" pin, Pull-up	WLAN Board ID bit0
6	BOARD_WLAN_ID1	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_1" pin, Pull-up	WLAN Board ID bit1
8	BOARD_WLAN_ID2	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_2" pin, Pull-up	WLAN Board ID bit2
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
3	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
4	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
5	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
31	VDD_WLAN_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
32	VDD_WLAN_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
33	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
34	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
7	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
12	GND	-	GND	GND	GND
23	GND	-	GND	GND	GND
30	GND	-	GND	GND	GND
36	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND
48	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description
59	GND	-	GND	GND	GND
9	TP	-	-	NC	-
10	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (GNSS IO voltage) on Control Board

1.3.2. WLAN Board Interface (Standard Reference Hardware)

Figure 3 shows the schematic of Control Board with WLAN CN that connects to WLAN Board for Standard Reference Hardware. Pin assignments of the connector (WLAN CN) and connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

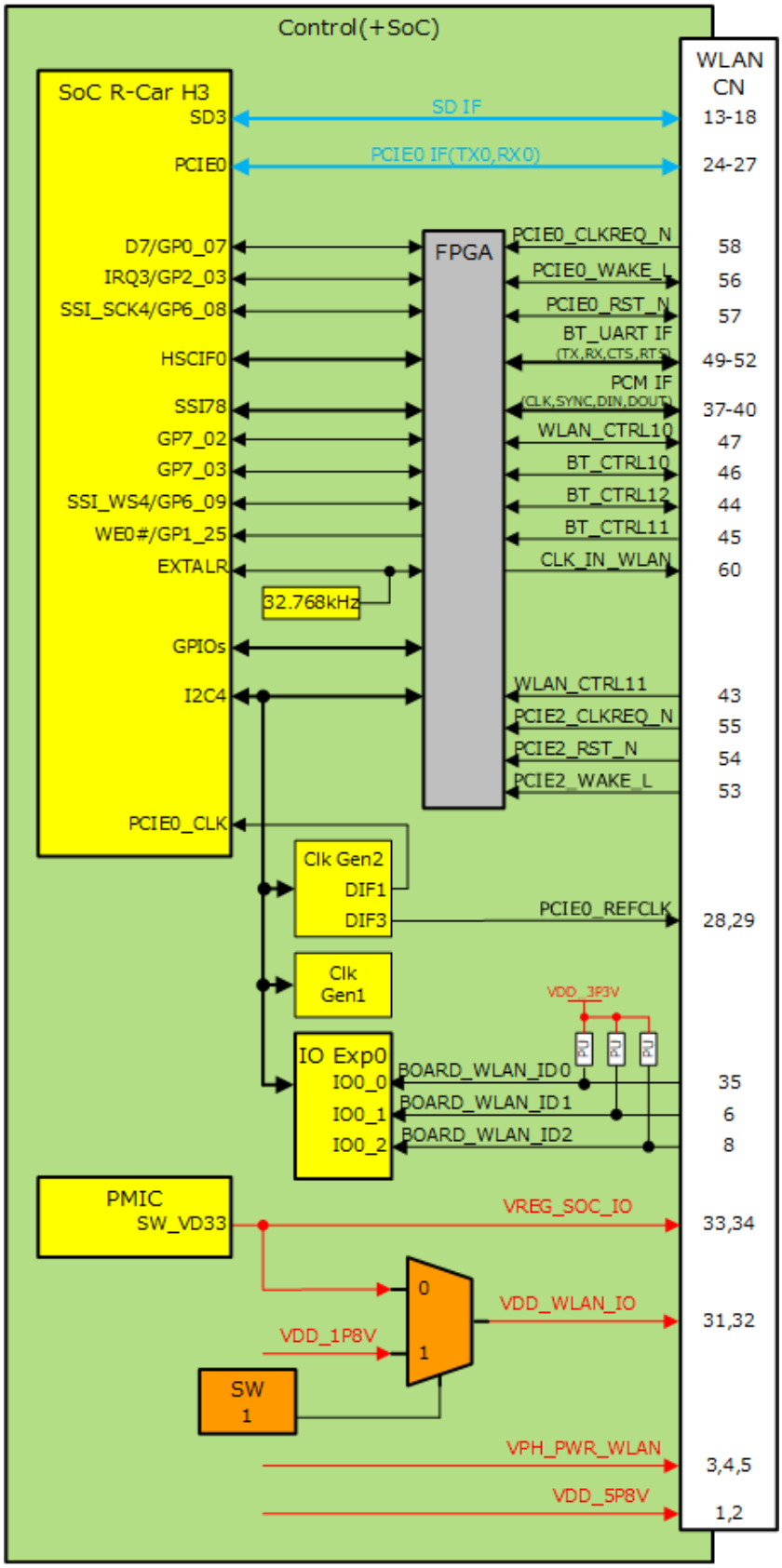


Figure 3 Connectivity between WLAN Board and Control Board (Standard Reference Hardware)

Table 3 Connector (WLAN CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description Example of use
25	PCIE0_TX0_P	>	LVDS	SoC PCIe ch0 Tx Data+(SoC Tx)	PCIe ch0 Tx Data+(SoC Tx)
24	PCIE0_TX0_M	>	LVDS	SoC PCIe ch0 Tx Data-(SoC Tx)	PCIe ch0 Tx Data-(SoC Tx)
27	PCIE0_RX0_P	<	LVDS	SoC PCIe ch0 Rx Data+(SoC Rx)	PCIe ch0 Rx Data+(SoC Rx)
26	PCIE0_RX0_M	<	LVDS	SoC PCIe ch0 Rx Data-(SoC Rx)	PCIe ch0 Rx Data-(SoC Rx)
29	PCIE0_REFCLK_P	>	LVDS	SoC PCIe ch0 Reference Clock+	PCIe ch0 Reference Clock+
28	PCIE0_REFCLK_M	>	LVDS	SoC PCIe ch0 Reference Clock-	PCIe ch0 Reference Clock-
56	PCIE0_WAKE_L	<	VCCIO_FPGA	FPGA	PCIe ch0 Wake Event
57	PCIE0_RST_N	>	VCCIO_FPGA	FPGA	PCIe ch0 Reset
58	PCIE0_CLKREQ_N	<	VCCIO_FPGA	FPGA	PCIe ch0 Clock Request
15	PCIE2_TX0_P	>	LVDS	SoC PCIe ch2 Tx0 Data+(SoC Tx)	PCIe ch2 Tx0 Data+(SoC Tx)
16	PCIE2_TX0_M	>	LVDS	SoC PCIe ch2 Tx0 Data-(SoC Tx)	PCIe ch2 Tx0 Data-(SoC Tx)
17	PCIE2_RX0_P	<	LVDS	SoC PCIe ch2 Rx0 Data+(SoC Rx)	PCIe ch2 Rx0 Data+(SoC Rx)
18	PCIE2_RX0_M	<	LVDS	SoC PCIe ch2 Rx0 Data-(SoC Rx)	PCIe ch2 Rx0 Data-(SoC Rx)
19	PCIE2_TX1_P	>	LVDS	SoC PCIe ch2 Tx1 Data+(SoC Tx)	PCIe ch2 Tx1 Data+(SoC Tx)
20	PCIE2_TX1_M	>	LVDS	SoC PCIe ch2 Tx1 Data-(SoC Tx)	PCIe ch2 Tx1 Data-(SoC Tx)
21	PCIE2_RX1_P	<	LVDS	SoC PCIe ch2 Rx1 Data+(SoC Rx)	PCIe ch2 Rx1 Data+(SoC Rx)
22	PCIE2_RX1_M	<	LVDS	SoC PCIe ch2 Rx1 Data-(SoC Rx)	PCIe ch2 Rx1 Data-(SoC Rx)
13	PCIE2_REFCLK_P	>	LVDS	SoC PCIe ch2 Reference Clock+	PCIe ch2 Reference Clock+
14	PCIE2_REFCLK_M	>	LVDS	SoC PCIe ch2 Reference Clock-	PCIe ch2 Reference Clock-
53	PCIE2_WAKE_L	<	VCCIO_FPGA	FPGA	PCIe ch2 Wake Event
54	PCIE2_RST_N	>	VCCIO_FPGA	FPGA	PCIe ch2 Reset
55	PCIE2_CLKREQ_N	<	VCCIO_FPGA	FPGA	PCIe ch2 Clock Request
60	CLK_IN_WLAN	>	VCCIO_FPGA	FPGA	Low-power clock input
47	WLAN_CTRL10	<>	VCCIO_FPGA	FPGA	GPIO, e.g. WLAN Enable(H:Enable)
43	WLAN_CTRL11	<>	VCCIO_FPGA	FPGA	GPIO
52	BT_UART_TX	>	VCCIO_FPGA	FPGA	Bluetooth UART Tx Data(SoC Tx)
51	BT_UART_RX	<	VCCIO_FPGA	FPGA	Bluetooth UART Rx Data(SoC Rx)
50	BT_UART_CTS	<	VCCIO_FPGA	FPGA	Bluetooth UART Control(SoC CTS)

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description Example of use
49	BT_UART_RTS	>	VCCIO_FPGA	FPGA	Bluetooth UART Control(SoC RTS)
37	PCM_CLK	>	VCCIO_FPGA	FPGA	Bluetooth PCM Clock
38	PCM_SYNC	>	VCCIO_FPGA	FPGA	Bluetooth PCM Sync
39	PCM_DIN	<	VCCIO_FPGA	FPGA	Bluetooth PCM Data In(SoC In)
40	PCM_DOUT	>	VCCIO_FPGA	FPGA	Bluetooth PCM Data Out(SoC Out)
46	BT_CTRL10	<>	VCCIO_FPGA	FPGA	GPIO, e.g. Bluetooth Enable(H:Enable)
45	BT_CTRL11	<>	VCCIO_FPGA	FPGA	GPIO, e.g. Bluetooth Wakeup host(H:Wakeup)
44	BT_CTRL12	<>	VCCIO_FPGA	FPGA	GPIO, e.g. Bluetooth RF front-end turn-off(L:OFF)
35	BOARD_WLAN_ID0	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_0" pin, Pull-up	WLAN Board ID bit0
6	BOARD_WLAN_ID1	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_1" pin, Pull-up	WLAN Board ID bit1
8	BOARD_WLAN_ID2	<	3.3[V]	IO Expander(PCA9539)-0 "IO0_2" pin, Pull-up	WLAN Board ID bit2
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
3	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
4	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
5	VPH_PWR_WLAN	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
31	VDD_WLAN_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
32	VDD_WLAN_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
33	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
34	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
7	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
12	GND	-	GND	GND	GND
23	GND	-	GND	GND	GND
30	GND	-	GND	GND	GND
36	GND	-	GND	GND	GND
41	GND	-	GND	GND	GND
42	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - WLAN	Voltage	Connection of the control board	Description Example of use
48	GND	-	GND	GND	GND
59	GND	-	GND	GND	GND
9	TP	-	-	NC	-
10	TP	-	-	NC	-

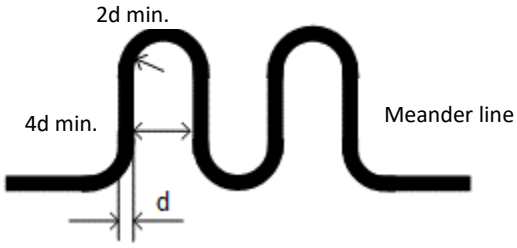
*1: Voltage depends on the power supply switch setting (GNSS IO voltage) on Control Board

1.4. Board Layout Consideration

Due to LVDS lines on Control Board, traces on WLAN Board need to be designed in accordance with the following restrictions:

PCI-Express Differential Signal

- Trace Length Matching: Difference between a differential signaling pair (+and -) must be 0.1[mm] maximum
- Difference between an average length of a clock pair (average of + signal and – signal)/a data signal pair : 0.1[mm] maximum.
- Maximum Trace Length : 30[mm]
- Differential Impedance : 85[Ω](85[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be at least twice the width of the trace. The gap between the meander traces should be at least four times the trace width.



Power Supply

- Comply with power supply requirements (impedance property, etc.) of the device to connect.
  If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[℃] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.

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