



Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

References

No.	Document Filename	Version	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

Contents

1. GNSS Board ..... 6

    1.1. Board Outline ..... 6

    1.2. Power Supply ..... 7

    1.3. Board-to-Board Interface ..... 7

        1.3.1. GNSS Board Interface (R-Car H3 Reference Hardware) ..... 8

        1.3.2. GNSS Board Interface (Standard Reference Hardware)..... 11

    1.4. Board Layout Consideration ..... 14

2. Disclaimer ..... 15

**Figures and Tables**

Figure 1 Board Dimension ..... 6

Figure 2 Connectivity between GNSS Board and Control Board (R-Car H3 Reference Hardware) ..... 8

Figure 3 Connectivity between GNSS Board and Control Board (Standard Reference Hardware) ..... 11

Table 1 GNSS Board Power Supply ..... 7

Table 2 Connector (GNSS CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware) 9

Table 3 Connector (GNSS CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)  
..... 12

## 1. GNSS Board

GNSS Board is connected to Control Board and communicates with the SoC to process information obtained from GNSS. The interfaces connected to the SoC in this document are analog signal, UART, and differential signal that one pair of differential clock signals and 4 signal pairs (total 5 pairs, 10 lines) but may vary depending on a SoC. Antennas can either be integrated onto GNSS Board or connected separately.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

### 1.1. Board Outline

The following figure shows GNSS Board dimension. 1.2[mm] is the assumed board thickness. If the change is required, interference with other boards should be considered.

The interface to Control Board is a 40-pin board-to-board connector mounted on the solder side of GNSS Board.

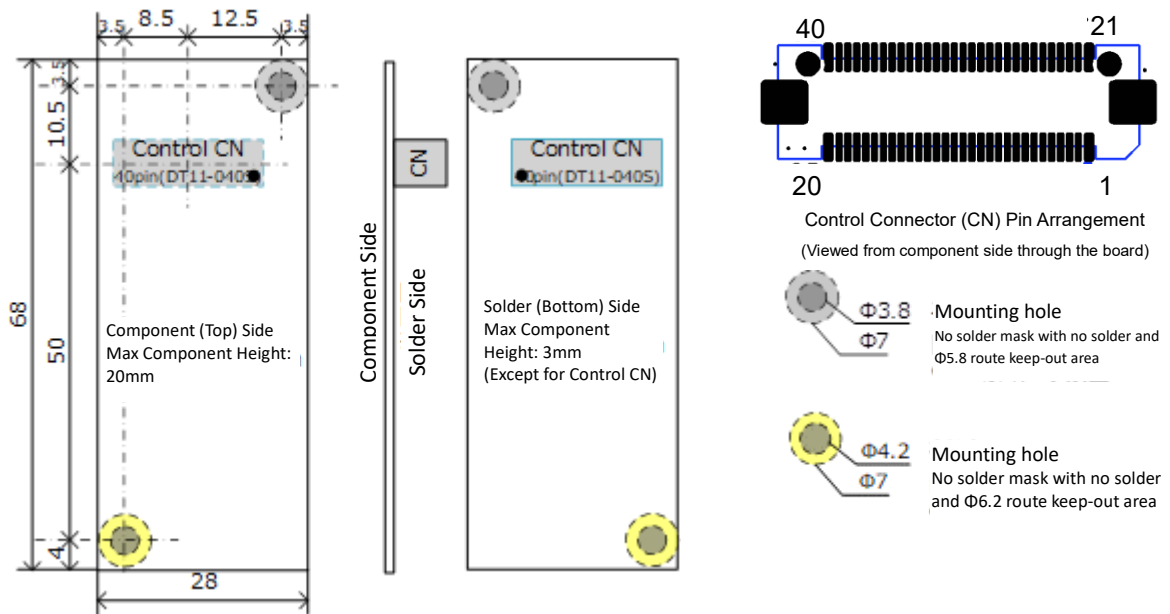


Figure 1 Board Dimension

### 1.2. Power Supply

There are four power supply rails that power GNSS Board. The specification of each power is shown in Table 1.

Table 1 GNSS Board Power Supply

Signal Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
VDD_5P8V		5.87		150	Pin 19, Pin 20 (2 pins)
VPH_PWR_GNSS		3.4 to 5.0		800	Pin 17, Pin 18 (2 pins) Voltage varies depending on a SoC The Voltage in R-Car H3 Reference Hardware is 5V
VDD_GNSS_IO		1.8 or 3.3		100	Pin 39, Pin 40 (2 pins) Voltage depends on the power supply switch setting on Control board. 3.3V is the default setting for R-Car H3 Reference Hardware
V IO_PF (VREG_SOC_IO)		SoC dependent		50	Pin 16 (1 pin)
VDD_GNSS_CORE		1.5		100	Pin 37, Pin 38 (2 pins)

A power circuit can be built on GNSS Board if no power source is available for an intended purpose.

Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, one of the possible solutions is to use another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards). Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins.

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

### 1.3. Board-to-Board Interface

40-pin board-to-board connector is used to connect Control Board to GNSS Board. A receptacle connector (KEL DT01-040S) is assumed to be used on the side of Control Board and a plug connector (KEL DT11-040S-10) is assumed to be used on the side of GNSS Board.

These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of  $\pm 0.5$  [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA]

The voltage for signals interfacing with Control Board should be able to adjust to both 1.8[V] and 3.3[V] as GNSS Board and WLAN Board uses signals of the same terminal voltage. The voltage level should be able to shift using such as a level shifter to make the voltage for signals consistent. When a signal output is on GNSS Board side and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.

A pull-up or pull-down resistor should be added to GNSS Board for the external resistor required for I2C signal, etc.

When connecting an antenna outside of the board enclosure, the antenna should be connected to Vehicle Board where internally placed GNSS Board is connected via a coaxial cable. A connector used for the coaxial cable is I-PEX's 20279-001E.

1.3.1. GNSS Board Interface (R-Car H3 Reference Hardware)

Figure 2 shows a schematic illustrating simplified connections between Control Board and GNSS Board for R-Car H3 Reference Hardware. Pin assignment of the connector (GNSS CN) and the connected terminals are listed on Table 2.

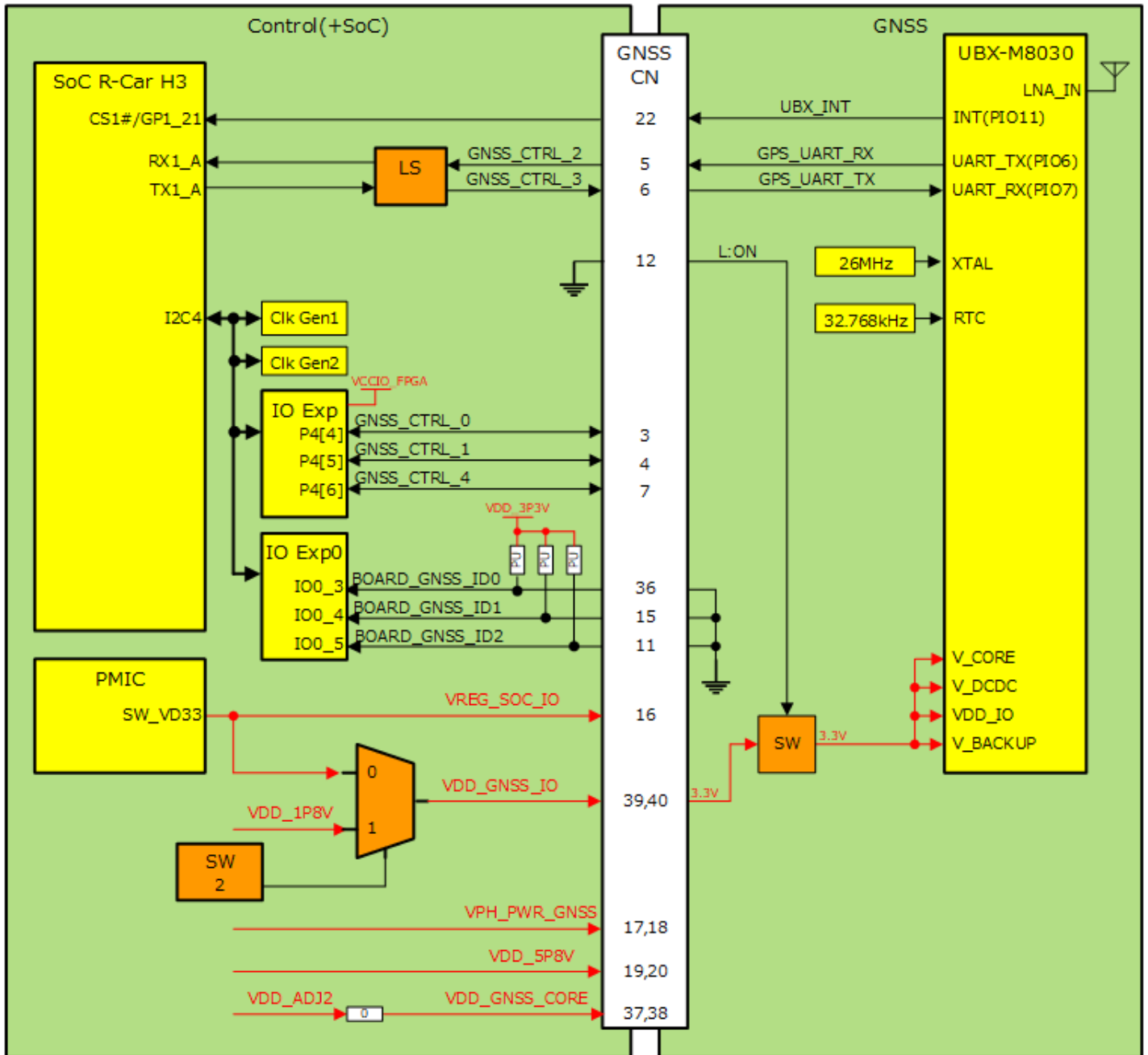


Figure 2 Connectivity between GNSS Board and Control Board (R-Car H3 Reference Hardware)



Table 2 Connector (GNSS CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - GNSS	Voltage	Connection of the control board	Description
33	GNSS_BB_I	-	-	NC	-
32	GNSS_BB_Q	-	-	NC	-
21	QLINK_UL0_P	-	-	NC	-
22	QLINK_UL0_M	<	3.3[V]	R-Car H3 "CS1#/GP1_21" pin	GNSS Interrupt
23	QLINK_UDL2_P	-	-	NC	-
24	QLINK_UDL2_M	-	-	NC	-
25	QLINK_UDL1_P	-	-	NC	-
26	QLINK_UDL1_M	-	-	NC	-
27	QLINK_DL0_P	-	-	NC	-
28	QLINK_DL0_M	-	-	NC	-
29	QLINK_CLK_P	-	-	NC	-
30	QLINK_CLK_M	-	-	NC	-
1	CLK_IN	-	-	No used	-
12	GPIO_077	>	3.3[V]	Fixed Low	GNSS Power Enable (L:ON)
3	GNSS_CTRL_0	<>	3.3[V]	IO Expander-4 bit4	No used
4	GNSS_CTRL_1	<>	3.3[V]	IO Expander-4 bit5	No used
5	GNSS_CTRL_2	<	3.3[V]	R-Car H3 "RX1_A" pin	GNSS UART Rx Data(SoC Rx)
6	GNSS_CTRL_3	>	3.3[V]	R-Car H3 "TX1_A" pin	GNSS UART Tx Data(SoC Tx)
7	GNSS_CTRL_4	<>	3.3[V]	IO Expander-4 bit6	No used
8	GNSS_CTRL_5	-	-	No used	-
9	GNSS_CTRL_6	-	-	No used	-
10	GNSS_CTRL_7	-	-	No used	-
36	BOARD_GNSS_ID0	<	3.3[V]	IO Expander(PC9539)-0 "IO0_3" pin, Pull-up	GNSS Board ID bit0
15	BOARD_GNSS_ID1	<	3.3[V]	IO Expander(PC9539)-0 "IO0_4" pin, Pull-up	GNSS Board ID bit1
11	BOARD_GNSS_ID2	<	3.3[V]	IO Expander(PC9539)-0 "IO0_5" pin, Pull-up	GNSS Board ID bit2
16	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
17	VPH_PWR_GNSS	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
18	VPH_PWR_GNSS	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power

## Reference Hardware Design Guideline for GNSS Board

Pin	Signal Name	Direction Control - GNSS	Voltage	Connection of the control board	Description
19	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
20	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
37	VDD_GNSS_CORE	>	Power:1.5[V]	1.5[V] output LDO	Power
38	VDD_GNSS_CORE	>	Power:1.5[V]	1.5[V] output LDO	Power
39	VDD_GNSS_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
40	VDD_GNSS_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
2	GND	-	GND	GND	GND
13	GND	-	GND	GND	GND
14	GND	-	GND	GND	GND
31	GND	-	GND	GND	GND
34	GND	-	GND	GND	GND
35	GND	-	GND	GND	GND

\*1: Voltage depends on the setting of the switched power supply (GNSS IO voltage) on Control Board.

1.3.2. GNSS Board Interface (Standard Reference Hardware)

Figure 3 shows the schematic of Control Board with GNSS CN that connects to GNSS Board for Standard Reference Hardware. Pin assignments of the connector (GNSS CN) and the connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

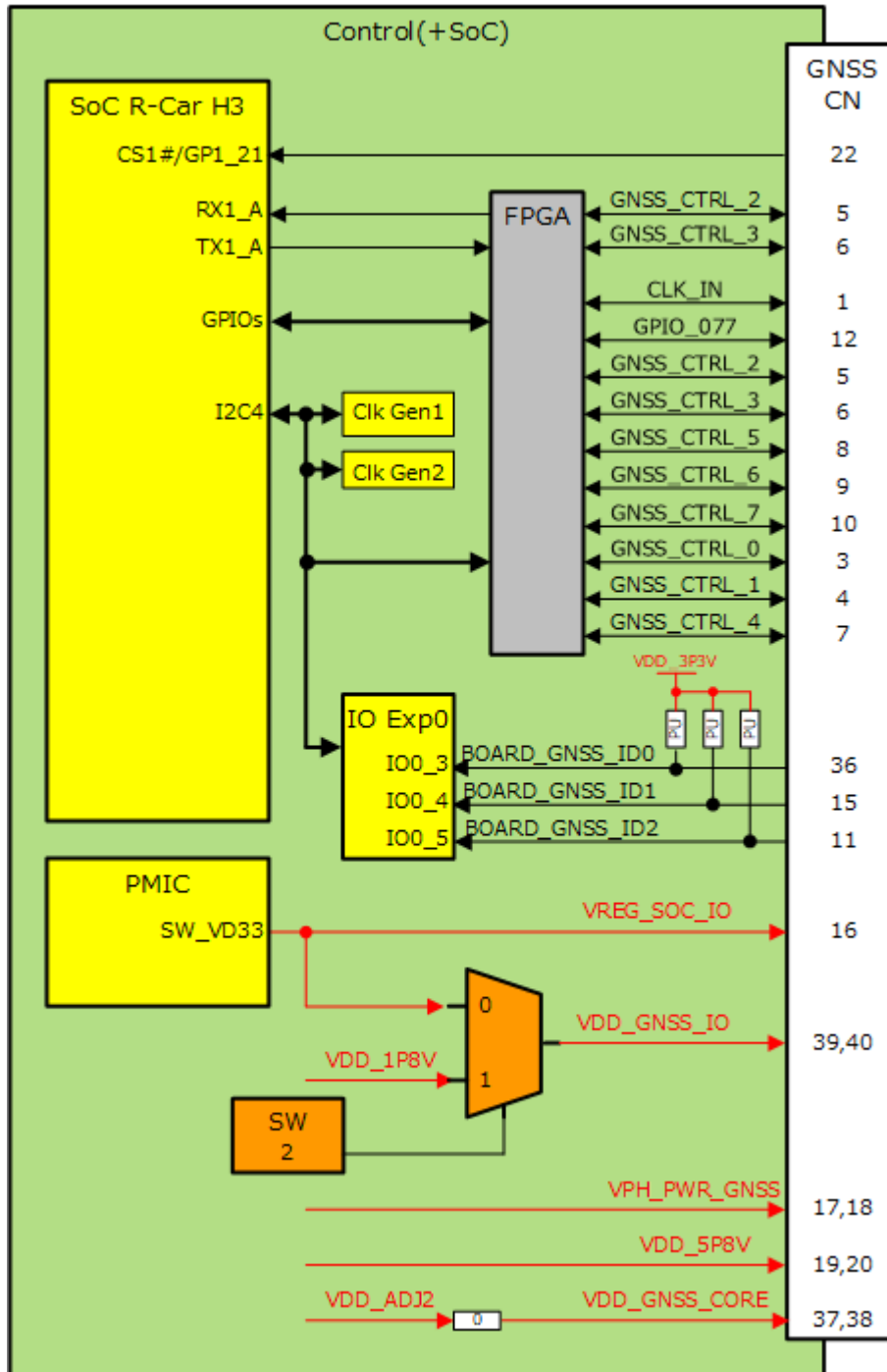


Figure 3 Connectivity between GNSS Board and Control Board (Standard Reference Hardware)

Table 3 Connector (GNSS CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - GNSS	Voltage	Connection of the control board	Description Example of use
33	GNSS_BB_I	-	-	NC	-
32	GNSS_BB_Q	-	-	NC	-
21	QLINK_UL0_P	-	-	NC	-
22	QLINK_UL0_M	<	VREG_SOC_IO	SoC GPIO pin	GPIO, e.g. GNSS Interrupt
23	QLINK_UDL2_P	-	-	NC	-
24	QLINK_UDL2_M	-	-	NC	-
25	QLINK_UDL1_P	-	-	NC	-
26	QLINK_UDL1_M	-	-	NC	-
27	QLINK_DL0_P	-	-	NC	-
28	QLINK_DL0_M	-	-	NC	-
29	QLINK_CLK_P	-	-	NC	-
30	QLINK_CLK_M	-	-	NC	-
1	CLK_IN	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS Clock
12	GPIO_077	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS Power Enable
3	GNSS_CTRL_0	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS UART Control(SoC UART CTS)
4	GNSS_CTRL_1	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS UART Control(SoC UART RTS)
5	GNSS_CTRL_2	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS UART Rx Data(SoC UART Rx)
6	GNSS_CTRL_3	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS UART Tx Data(SoC UART Tx)
7	GNSS_CTRL_4	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS Reset
8	GNSS_CTRL_5	<>	VCCIO_FPGA	FPGA	GPIO, e.g. GNSS Antenna Detect
9	GNSS_CTRL_6	<>	VCCIO_FPGA	FPGA	GPIO
10	GNSS_CTRL_7	<>	VCCIO_FPGA	FPGA	GPIO
36	BOARD_GNSS_ID0	<	3.3[V]	IO Expander(PC9539)-0 "IO0_3" pin, Pull-up	GNSS Board ID bit0
15	BOARD_GNSS_ID1	<	3.3[V]	IO Expander(PC9539)-0 "IO0_4" pin, Pull-up	GNSS Board ID bit1
11	BOARD_GNSS_ID2	<	3.3[V]	IO Expander(PC9539)-0 "IO0_5" pin, Pull-up	GNSS Board ID bit2
16	VREG_SOC_IO	>	Power:3.3[V]	3.3[V] output PMIC (SoC IO power)	Power
17	VPH_PWR_GNSS	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power
18	VPH_PWR_GNSS	>	Power:5.0[V]	5.0[V] output DCDC through switch	Power

## Reference Hardware Design Guideline for GNSS Board

Pin	Signal Name	Direction Control - GNSS	Voltage	Connection of the control board	Description Example of use
19	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
20	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
37	VDD_GNSS_CORE	>	Power:1.5[V]	1.5[V] output LDO	Power
38	VDD_GNSS_CORE	>	Power:1.5[V]	1.5[V] output LDO	Power
39	VDD_GNSS_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
40	VDD_GNSS_IO	>	Power:3.3[V] *1	3.3[V] output PMIC (SoC IO power)	Power
2	GND	-	GND	GND	GND
13	GND	-	GND	GND	GND
14	GND	-	GND	GND	GND
31	GND	-	GND	GND	GND
34	GND	-	GND	GND	GND
35	GND	-	GND	GND	GND

\*1: Voltage depends on the power supply switch setting (GNSS IO voltage) on Control Board.

### 1.4. Board Layout Consideration

The GNSS Board design should comply with specifications relevant to GNSS IC wiring and design guidelines. LVDS line on the side of Control Board is designed to attain 100 [ $\Omega$ ] differential impedance.

### 2. Disclaimer

1. This document is provided only as a reference material to properly use the AGL reference hardware, and there are no guarantee and no rights granted or executed of Panasonic's and or others' intellectual property rights and other rights regarding any technical information described in this document.
2. Panasonic disclaims any and all liability for any losses, damages and infringement of any third parties' intellectual property rights and other rights incurred by AGL and/or any third parties arising from the use of these product data, figures, tables, or any and all information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Panasonic or others.
3. AGL has a rights to copy this document solely for the purpose of use the AGL reference hardware, but any other rights (e.g., modification of this document) is subject to Panasonic's prior written consent. Notwithstanding the foregoing, Panasonic disclaims any and all liability for any losses, damages and infringement of any third parties' intellectual property rights and any other rights incurred by AGL or any third parties arising from the use of any copied and any modified documents.
4. AGL shall not use the products and technologies described in this document, directly or indirectly, for Military Purposes which is the design, development, manufacture, storage or use of any weapons, including, without limitation, nuclear weapons, chemical weapons, biological weapons and missiles. If any of the products or technical information described in this document is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.
5. All information such as product data, figures or tables described in this document is as of the released date of this document, and Panasonic may change the product and/or its specification without notice.
6. All information described in this document has been carefully prepared with reasonable care, but any errors may be contained in this document. Panasonic shall not be liable for any losses, any damages incurred by AGL and/or any third parties arising from any error, bugs or faults of this document.
7. The products described in this document are intended to be used for general applications (such as entertainment, air conditioning, communications, measuring), and should not be used for Special Applications (such as for airplanes, aerospace, automotive driving equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body. It is to be understood that Panasonic shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this document for any Special Application.
8. Unless otherwise permitted by Panasonic or applicable Law, AGL shall not alter, modify, copy, or reverse engineer AGL Reference Hardware, whether in whole or in part. Panasonic disclaims any and all liability for any losses or damages incurred by AGL or third parties arising from such alteration, modification, copying or reverse engineering.
9. The product described in this document has a structure that can be easily disassembled, and there is a danger of accidents such as infants accidentally swallowing it by putting it in the mouth when any parts are removed from the product. Please take sufficient safety measures at your own risk to prevent such events from occurring. Panasonic is not liable for any accidents that occur due to such parts removed from the product by AGL.
10. The products described in this document is NOT designed to comply with any such as the environmental compatibility and Electro-Magnetic Compatibility of products. Panasonic is not liable for any damages caused by your non-compliance with applicable laws or regulations.
11. AGL shall be responsible to cause any members of AGL to comply with any terms and conditions described in this notice.

#### Regarding Software;

The provided patch files, yocto recipes and other files included in the AGL\_Refhw\_sample\_software\_yyyyymmdd.tar.gz are

- (1) developed by Panasonic Corporation ("Panasonic"),
- (2) licensed under the GNU GENERAL PUBLIC LICENSE, Version 2 ("GPL"), and/or
- (3) open sourced software licensed under terms and conditions other than GPL.

We shall not be responsible or liable for any loss or damage that may occur due to the use of these files.