Reference Hardware Design Guideline

VideoIn Board

Version	Date
1.0	May 25, 2020

Panasonic Corporation

Automotive Company R&D Division

Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

References

No.	Document	Version	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

Contents

Figures and Tables

1. VideoIn Board

VideoIn Board is connected to Control Board and receives image signals from cameras, etc. There are 3 from VideoIn0 to VideoIn2 and a maximum of 3 boards can be connected to use concurrently. 1 pair of differential clock signal and 4 pairs of data signal as 1 channel (total 5 pairs=10 lines) is connected as an interface with image data to SoC.

A SoC can assign signals required for image output to VideoIn1 to which a board for both image input and output can be connected. In addition, VideoIn0 adds 1 channel of differential signal to SoC.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3 (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”)

1.1. Board Outline

The following figure shows VideoIn Board dimension. 1.2[mm] is the assumed thickness, but if the design modification is required, special attention should be paid to avoid the interference with other boards.

The interface to Control Board is a 60-pin board-to-board connector mounted on the solder side of VideoIn Board. The external interface connectors are also mounted on the solder side so as to avoid the interference with another board when assembled.

The spacing between the board and chassis is shown as below. External interface connectors are to be placed in the position relative to the chassis.

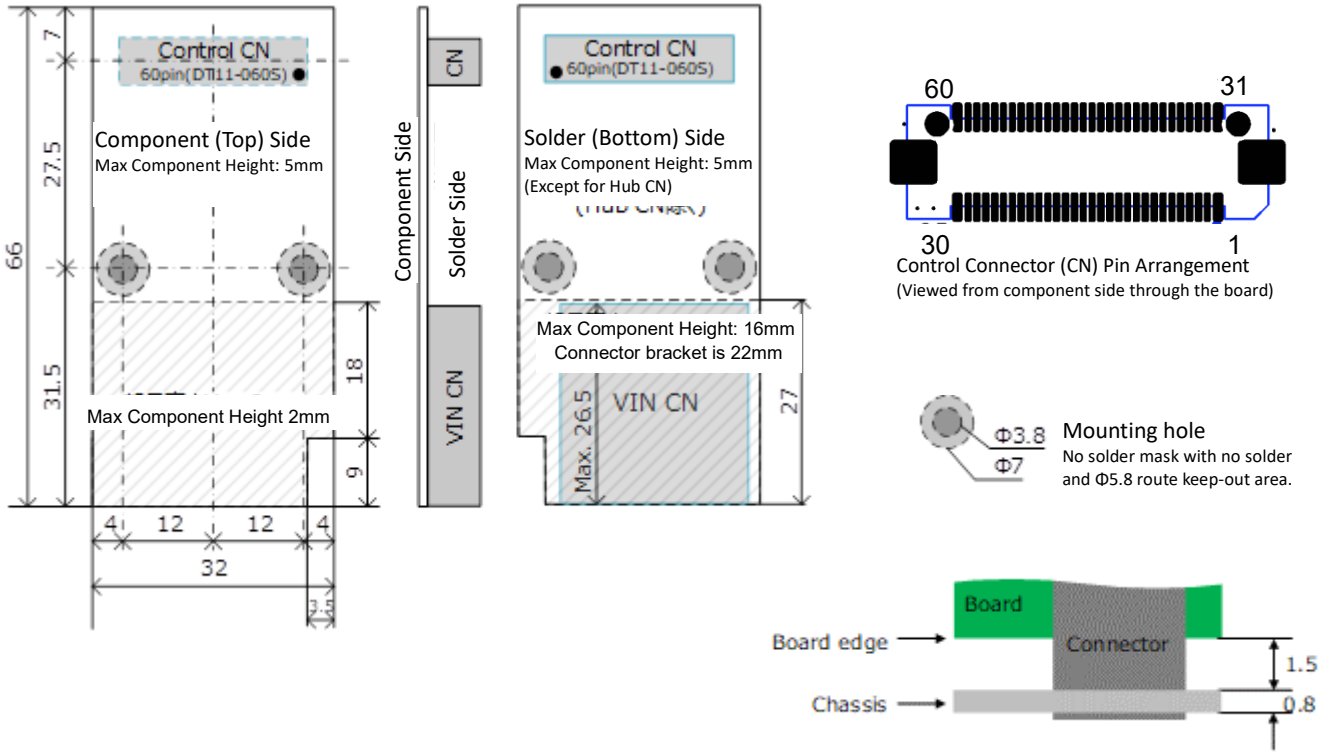


Figure 1 VideoIn Board Dimension

The space for two boards can be used if more space is required.

Either one of the following combinations is applicable.

VideoIn1 (CN1 on Figure 2) +VideoIn0 (CN2 on Figure 2)

VideoIn2 (CN1 on Figure 2) +VideoIn1 (CN2 on Figure 2)

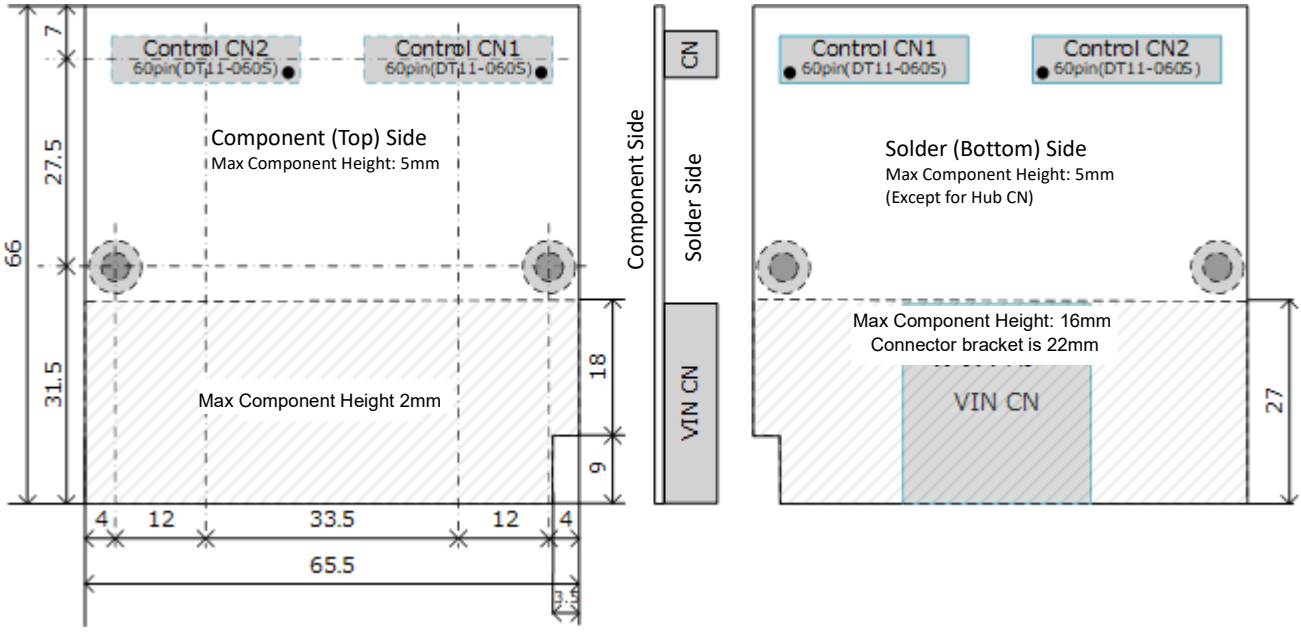


Figure 2 Expanded Board Dimension

1.2. Power Supply

There are four power rails to power VideoIn Board. Each power supply is specified as below.

Table 1 VideoIn Board Power Supply

Power Supply Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
VDD_5P8V		5.87		200	Pin 1,Pin 2 (2 pins)
VDD_3P3V		3.3		200	Pin 31, Pin 32 (2 pins)
VDD_1P8V		1.8		200	Pin 3, Pin 4 (2 pins)
VDD_IN_CORE		1.2/1.5		100	Pin 33, Pin 34 (2 pins) Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board. The voltages of all the three rails, VideoOut0-2, are changed when setting the switch. 1.5V is the default setting for R-Car H3 Reference Hardware

A power circuit can be built on VideoIn Board if no power source is available for an intended purpose.
Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, it is possible to supplement the amount with another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards), or expanding the board is also another option so that power supply is available from two connectors. Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins.

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

1.3. Board-to-Board Interface

60-pin board-to-board connectors is used to connect Control Board to VideoIn Board. A receptacle connector (KEL DT01-060S) is assumed to be used on the side of Control board, and a plug connector (KEL DT11-060S-10) is assumed to be used on the side of VideoIn Board.
These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of ±0.5 [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA].

Either 1.8[V] or 3.3[V] should be applied for signals interfacing with Control board as there are a variety of boards might be used for VideoIn Board simultaneously. The voltage applied to the signals should be able to manage to a consistent level using a level shifter. When a signal output is on VideoIn side and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.
A pull-up or pull-down resistor should be added to VideoIn Board for the external resistor required for I2C signal, etc.

1.3.1. VideoIn0 Board Interface (R-Car H3 Reference Hardware)

Figure 3 shows a schematic illustrating simplified connections between Control Board and VideoIn0 Board in R-Car H3 Reference Hardware. Connector (VIN0 CN) pin assignments and connected terminals are listed on Table 2.

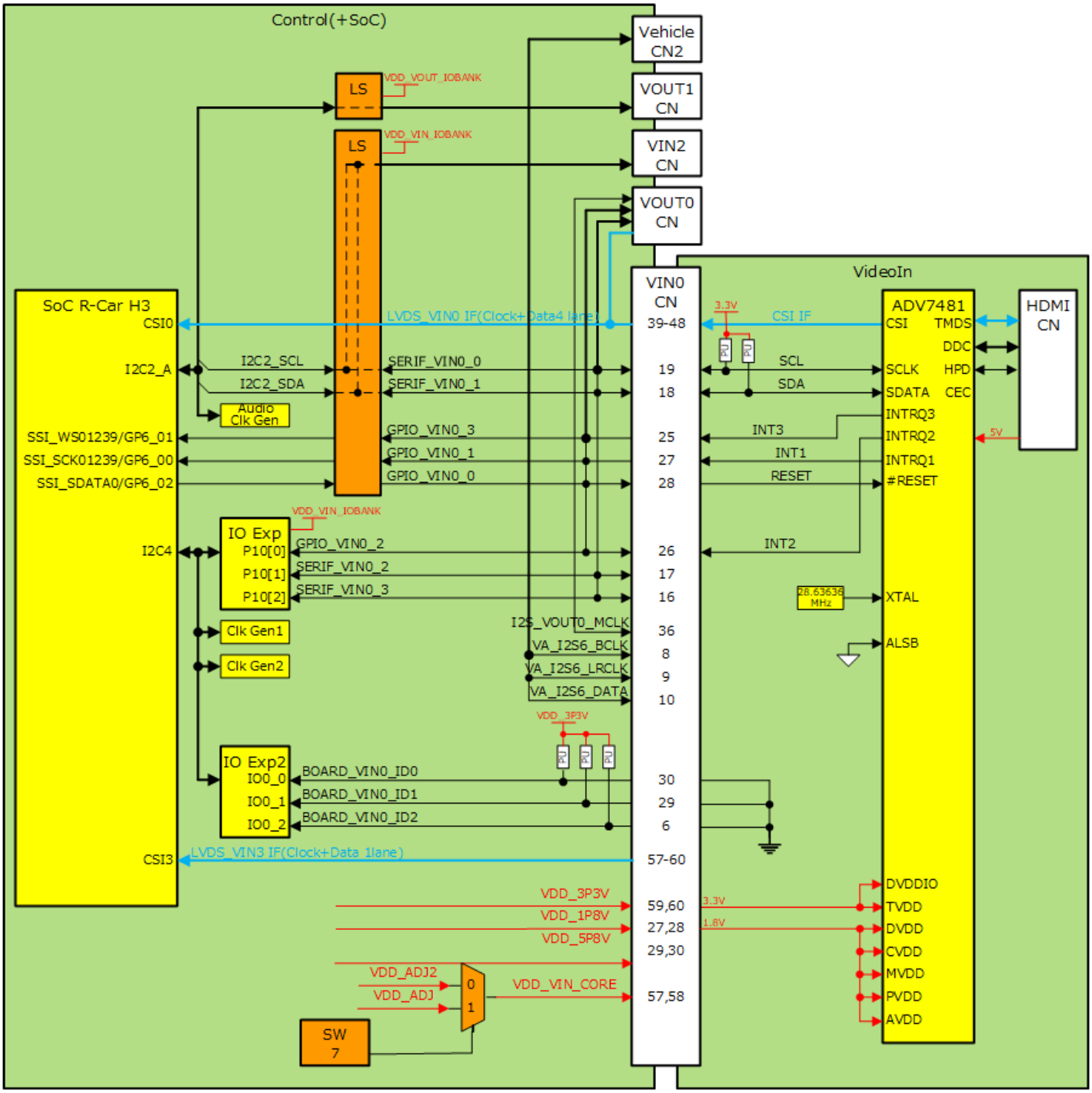


Figure 3 Connectivity between VideoIn0 Board and Control Board (R-Car H3 Reference Hardware)

Table 2 Connector (VIN0 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description
60	LVDS_IN3_CLK_P	<	LVDS	R-Car H3 "CSI3_CLKP" pin	No used
59	LVDS_IN3_CLK_M	<	LVDS	R-Car H3 "CSI3_CLKN" pin	No used
58	LVDS_IN3_LN0_P	<	LVDS	R-Car H3 "CSI3_DATAP0" pin	No used
57	LVDS_IN3_LN0_M	<	LVDS	R-Car H3 "CSI3_DATAN0" pin	No used
56	LVDS_IN3_LN1_P	-	-	NC	-
55	LVDS_IN3_LN1_M	-	-	NC	-
54	LVDS_IN3_LN2_P	-	-	NC	-
53	LVDS_IN3_LN2_M	-	-	NC	-
52	LVDS_IN3_LN3_P	-	-	NC	-
51	LVDS_IN3_LN3_M	-	-	NC	-
48	LVDS_IN0_CLK_P	<	LVDS	R-Car H3 "CSI0_CLKP" pin	CSI ch0 Clock+ (HDMI In to CSI Bridge)
47	LVDS_IN0_CLK_M	<	LVDS	R-Car H3 "CSI0_CLKN" pin	CSI ch0 Clock- (HDMI In to CSI Bridge)
46	LVDS_IN0_LN0_P	<	LVDS	R-Car H3 "CSI0_DATAP0" pin	CSI ch0 Data0+ (HDMI In to CSI Bridge)
45	LVDS_IN0_LN0_M	<	LVDS	R-Car H3 "CSI0_DATAN0" pin	CSI ch0 Data0- (HDMI In to CSI Bridge)
44	LVDS_IN0_LN1_P	<	LVDS	R-Car H3 "CSI0_DATAP1" pin	CSI ch0 Data1+ (HDMI In to CSI Bridge)
43	LVDS_IN0_LN1_M	<	LVDS	R-Car H3 "CSI0_DATAN1" pin	CSI ch0 Data1- (HDMI In to CSI Bridge)
42	LVDS_IN0_LN2_P	<	LVDS	R-Car H3 "CSI0_DATAP2" pin	CSI ch0 Data2+ (HDMI In to CSI Bridge)
41	LVDS_IN0_LN2_M	<	LVDS	R-Car H3 "CSI0_DATAN2" pin	CSI ch0 Data2- (HDMI In to CSI Bridge)
40	LVDS_IN0_LN3_P	<	LVDS	R-Car H3 "CSI0_DATAP3" pin	CSI ch0 Data3+ (HDMI In to CSI Bridge)
39	LVDS_IN0_LN3_M	<	LVDS	R-Car H3 "CSI0_DATAN3" pin	CSI ch0 Data3- (HDMI In to CSI Bridge)
24	VDI10	-	-	NC	-
23	VDI11	-	-	NC	-
22	VDI12	-	-	NC	-
21	VDI13	-	-	NC	-
28	GPIO_VIN0_0	>	3.3[V] *2	R-Car H3 "SSI_SDATA0/GP6_02" pin	HDMI In to CSI Bridge Reset
27	GPIO_VIN0_1	<	3.3[V] *2	R-Car H3 "SSI_SCK01239/GP6_00" pin	HDMI In to CSI Bridge INTRQ1
26	GPIO_VIN0_2	<>	3.3[V] *2	IO Expander-10 bit0	No used
25	GPIO_VIN0_3	<	3.3[V] *2	R-Car H3 "SSI_WS01239/GP6_01" pin	HDMI In to CSI Bridge INTRQ3

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description
15	VDI_VSYNC	-	-	NC	-
14	VDI_HSYNC	-	-	NC	-
13	VDI_FIELD	-	-	NC	-
12	VDI_CLK	-	-	NC	-
19	SERIF_VIN0_0	<>	3.3[V] *2	R-Car H3 "RTS0#/SCL2_A" pin	HDMI In to CSI Bridge SCLK
18	SERIF_VIN0_1	<>	3.3[V] *2	R-Car H3 "SCK0/SDA2_A" pin	HDMI In to CSI Bridge SDATA
17	SERIF_VIN0_2	<>	3.3[V] *2	IO Expander-10 bit1	No used
16	SERIF_VIN0_3	<>	3.3[V] *2	IO Expander-10 bit2	No used
10	VA_I2S6_DATA	-	-	No used	-
9	VA_I2S6_LRCLK	-	-	No used	-
8	VA_I2S6_BCLK	-	-	No used	-
36	I2S_VOUT0_MCLK	-	-	No used	-
30	BOARD_VIN0_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_0" pin, Pull-up	VideoIn0 Board ID bit0
29	BOARD_VIN0_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_1" pin, Pull-up	VideoIn0 Board ID bit1
6	BOARD_VIN0_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_2" pin, Pull-up	VideoIn0 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND
50	GND	-	GND	GND	GND
49	GND	-	GND	GND	GND
38	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description
37	GND	-	GND	GND	GND
5	GPANA_01	-	-	NC	-
35	GPANA_02	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control Board

1.3.2. VideoIn0 Board Interface (Standard Reference Hardware)

Figure 4 shows a schematic of Control Board with VIN0 CN that connects to VideoIn0 Board in Standard Reference Hardware. Pin assignments of the connector (VIN0 CN) and connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

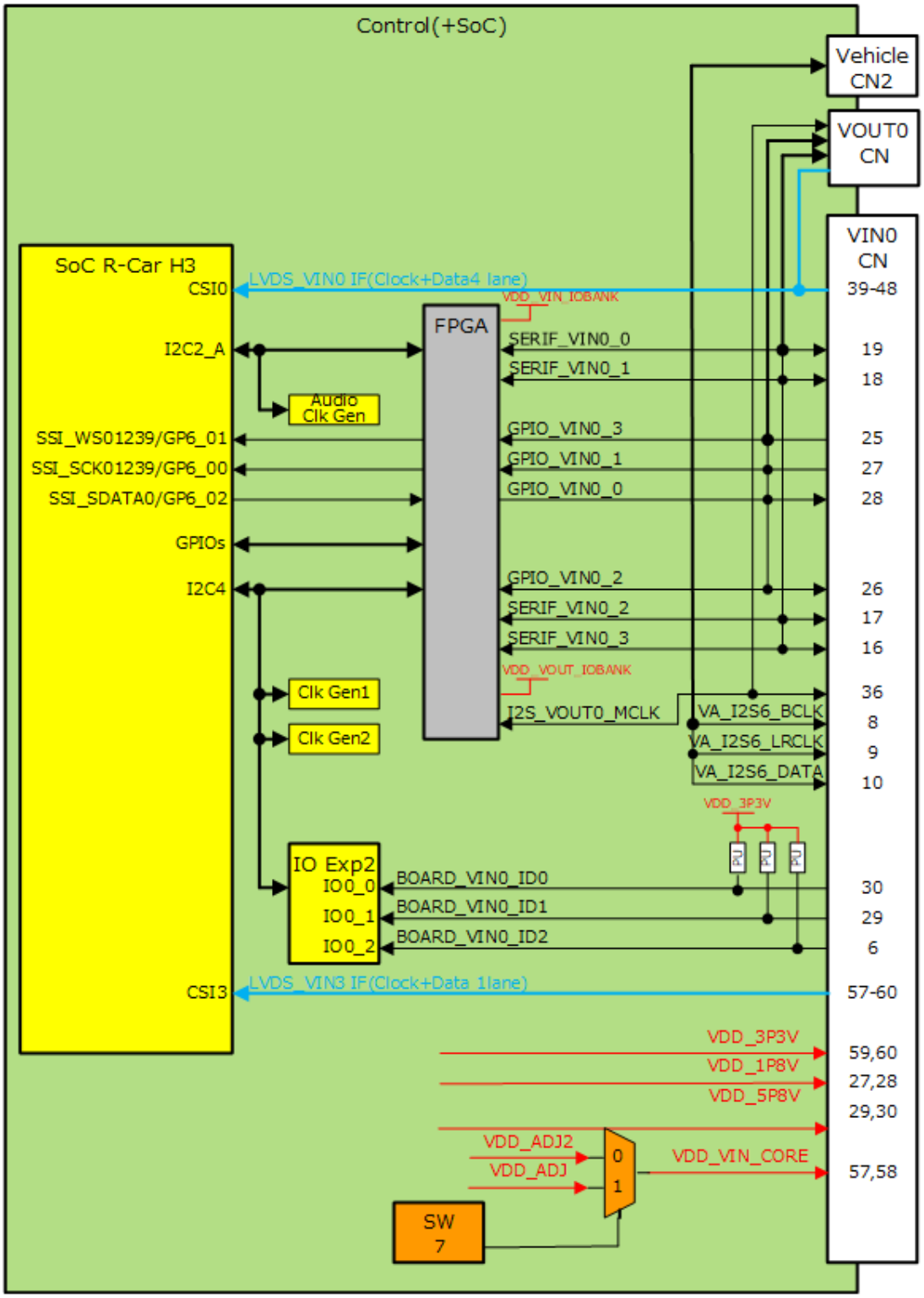


Figure 4 Connectivity between VideoIn0 Board and Control Board (Standard Reference Hardware)

Table 3 Connector (VIN0 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description Example of use
60	LVDS_IN3_CLK_P	<	LVDS	SoC VideoIn LVDS ch3 Clock+	SoC VideoIn LVDS ch3 Clock+
59	LVDS_IN3_CLK_M	<	LVDS	SoC VideoIn LVDS ch3 Clock-	SoC VideoIn LVDS ch3 Clock-
58	LVDS_IN3_LN0_P	<	LVDS	SoC VideoIn LVDS ch3 Data0+	SoC VideoIn LVDS ch3 Data0+
57	LVDS_IN3_LN0_M	<	LVDS	SoC VideoIn LVDS ch3 Data0-	SoC VideoIn LVDS ch3 Data0-
56	LVDS_IN3_LN1_P	<	LVDS	SoC VideoIn LVDS ch3 Data1+	SoC VideoIn LVDS ch3 Data1+
55	LVDS_IN3_LN1_M	<	LVDS	SoC VideoIn LVDS ch3 Data1-	SoC VideoIn LVDS ch3 Data1-
54	LVDS_IN3_LN2_P	<	LVDS	SoC VideoIn LVDS ch3 Data2+	SoC VideoIn LVDS ch3 Data2+
53	LVDS_IN3_LN2_M	<	LVDS	SoC VideoIn LVDS ch3 Data2-	SoC VideoIn LVDS ch3 Data2-
52	LVDS_IN3_LN3_P	<	LVDS	SoC VideoIn LVDS ch3 Data3+	SoC VideoIn LVDS ch3 Data3+
51	LVDS_IN3_LN3_M	<	LVDS	SoC VideoIn LVDS ch3 Data3-	SoC VideoIn LVDS ch3 Data3-
48	LVDS_IN0_CLK_P	<	LVDS	SoC VideoIn LVDS ch0 Clock+	SoC VideoIn LVDS ch0 Clock+
47	LVDS_IN0_CLK_M	<	LVDS	SoC VideoIn LVDS ch0 Clock-	SoC VideoIn LVDS ch0 Clock-
46	LVDS_IN0_LN0_P	<	LVDS	SoC VideoIn LVDS ch0 Data0+	SoC VideoIn LVDS ch0 Data0+
45	LVDS_IN0_LN0_M	<	LVDS	SoC VideoIn LVDS ch0 Data0-	SoC VideoIn LVDS ch0 Data0-
44	LVDS_IN0_LN1_P	<	LVDS	SoC VideoIn LVDS ch0 Data1+	SoC VideoIn LVDS ch0 Data1+
43	LVDS_IN0_LN1_M	<	LVDS	SoC VideoIn LVDS ch0 Data1-	SoC VideoIn LVDS ch0 Data1-
42	LVDS_IN0_LN2_P	<	LVDS	SoC VideoIn LVDS ch0 Data2+	SoC VideoIn LVDS ch0 Data2+
41	LVDS_IN0_LN2_M	<	LVDS	SoC VideoIn LVDS ch0 Data2-	SoC VideoIn LVDS ch0 Data2-
40	LVDS_IN0_LN3_P	<	LVDS	SoC VideoIn LVDS ch0 Data3+	SoC VideoIn LVDS ch0 Data3+
39	LVDS_IN0_LN3_M	<	LVDS	SoC VideoIn LVDS ch0 Data3-	SoC VideoIn LVDS ch0 Data3-
24	VDI10	-	-	NC	-
23	VDI11	-	-	NC	-
22	VDI12	-	-	NC	-
21	VDI13	-	-	NC	-
28	GPIO_VIN0_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Reset
27	GPIO_VIN0_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt
26	GPIO_VIN0_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Enable

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description Example of use
25	GPIO_VIN0_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt
15	VDI_VSYNC	-	-	NC	-
14	VDI_HSYNC	-	-	NC	-
13	VDI_FIELD	-	-	NC	-
12	VDI_CLK	-	-	NC	-
19	SERIF_VIN0_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
18	SERIF_VIN0_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
17	SERIF_VIN0_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
16	SERIF_VIN0_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
10	VA_I2S6_DATA	<>	IO_AUDIO	Vehicle CN2 90pin	No used, I2S ch6 Data
9	VA_I2S6_LRCLK	<>	IO_AUDIO	Vehicle CN2 91pin	No used, I2S ch6 LR Clock
8	VA_I2S6_BCLK	<>	IO_AUDIO	Vehicle CN2 92pin	No used, I2S ch6 Bit Clock
36	I2S_VOUT0_MCLK *2	<>	VDD_VOUT_IOBANK	FPGA	GPIO, e.g. I2S Master Clock
30	BOARD_VIN0_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_0" pin, Pull-up	VideoIn0 Board ID bit0
29	BOARD_VIN0_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_1" pin, Pull-up	VideoIn0 Board ID bit1
6	BOARD_VIN0_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_2" pin, Pull-up	VideoIn0 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN0	Voltage	Connection of the control board	Description Example of use
50	GND	-	GND	GND	GND
49	GND	-	GND	GND	GND
38	GND	-	GND	GND	GND
37	GND	-	GND	GND	GND
5	GPANA_01	<	-	SoC CN1 156pin	No used(Analog In1)
35	GPANA_02	<	-	SoC CN1 156pin	No used(Analog In2)

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board

*2: The signal is connected to VideoOut0 as well. If used on VideoOut0 Board, output conflict should be avoided.

1.3.3. VideoIn1 Board Interface (R-Car H3 Reference Hardware)

Figure 5 shows a schematic illustrating simplified connections between Control Board and VideoIn1 Board in R-Car H3 Reference Hardware. Connector (VIN1 CN) pin assignments and connected terminals are listed on Table 4.

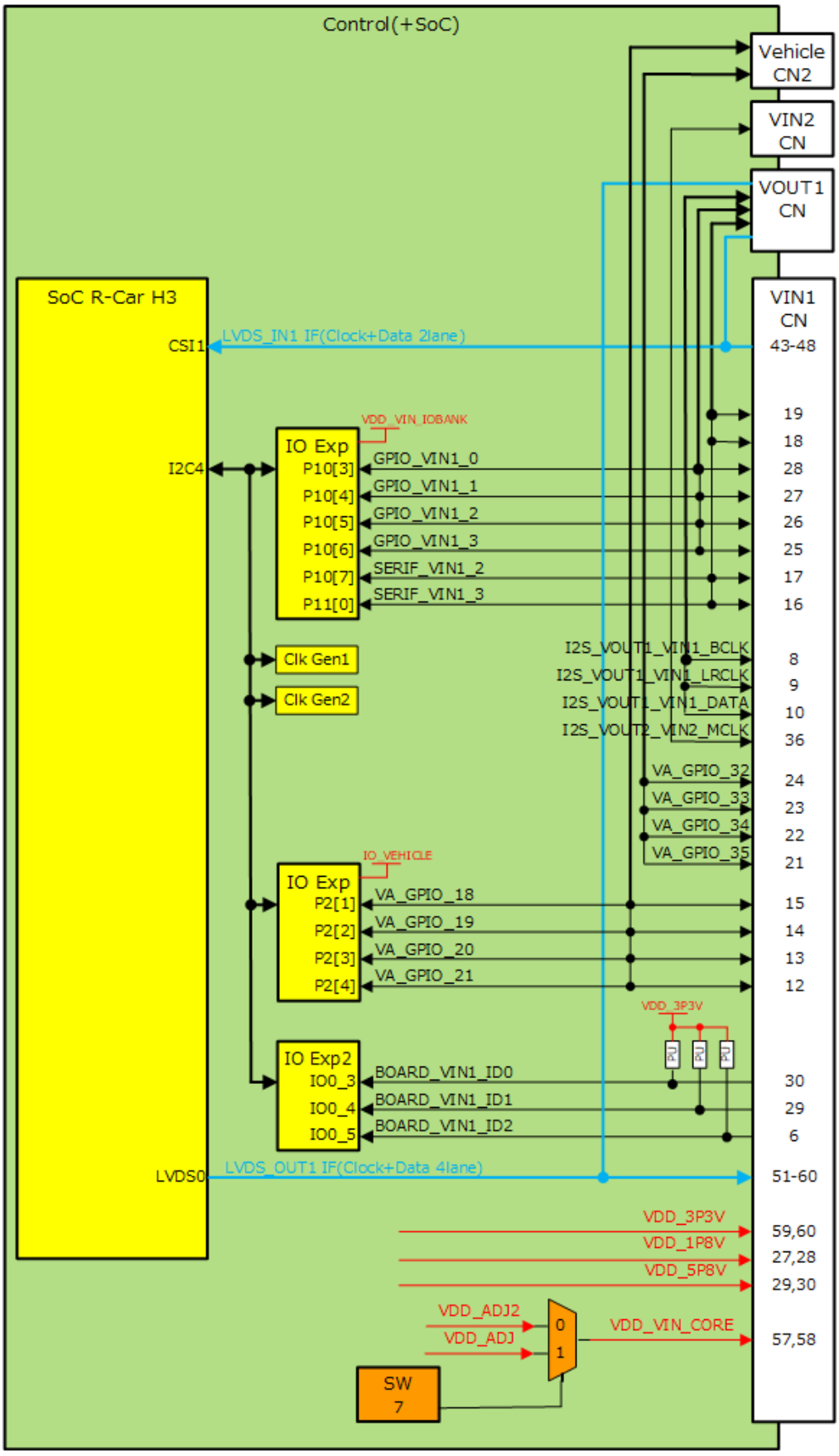


Figure 5 Connectivity between VideoIn1 Board and Control Board (R-Car H3 Reference Hardware)

Table 4 Connector (VIN1 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description
60	LVDS_OUT1_CLK_P	>	LVDS	R-Car H3 "LVDS0_CLK_P" pin	No used
59	LVDS_OUT1_CLK_M	>	LVDS	R-Car H3 "LVDS0_CLK_N" pin	No used
58	LVDS_OUT1_LN0_P	>	LVDS	R-Car H3 "LVDS0_CH0_P" pin	No used
57	LVDS_OUT1_LN0_M	>	LVDS	R-Car H3 "LVDS0_CH0_N" pin	No used
56	LVDS_OUT1_LN1_P	>	LVDS	R-Car H3 "LVDS0_CH1_P" pin	No used
55	LVDS_OUT1_LN1_M	>	LVDS	R-Car H3 "LVDS0_CH1_N" pin	No used
54	LVDS_OUT1_LN2_P	>	LVDS	R-Car H3 "LVDS0_CH2_P" pin	No used
53	LVDS_OUT1_LN2_M	>	LVDS	R-Car H3 "LVDS0_CH2_N" pin	No used
52	LVDS_OUT1_LN3_P	>	LVDS	R-Car H3 "LVDS0_CH3_P" pin	No used
51	LVDS_OUT1_LN3_M	>	LVDS	R-Car H3 "LVDS0_CH3_N" pin	No used
48	LVDS_IN1_CLK_P	<	LVDS	R-Car H3 "CSI1_CLKP" pin	No used
47	LVDS_IN1_CLK_M	<	LVDS	R-Car H3 "CSI1_CLKN" pin	No used
46	LVDS_IN1_LN0_P	<	LVDS	R-Car H3 "CSI1_DATAP0" pin	No used
45	LVDS_IN1_LN0_M	<	LVDS	R-Car H3 "CSI1_DATAN0" pin	No used
44	LVDS_IN1_LN1_P	<	LVDS	R-Car H3 "CSI1_DATAP1" pin	No used
43	LVDS_IN1_LN1_M	<	LVDS	R-Car H3 "CSI1_DATAN1" pin	No used
42	LVDS_IN1_LN2_P	-	-	NC	-
41	LVDS_IN1_LN2_M	-	-	NC	-
40	LVDS_IN1_LN3_P	-	-	NC	-
39	LVDS_IN1_LN3_M	-	-	NC	-
24	VA_GPIO_32	-	-	No used	-
23	VA_GPIO_33	-	-	No used	-
22	VA_GPIO_34	-	-	No used	-
21	VA_GPIO_35	-	-	No used	-
28	GPIO_VIN1_0	<>	3.3[V] *2	IO Expander-10 bit3	No used
27	GPIO_VIN1_1	<>	3.3[V] *2	IO Expander-10 bit4	No used
26	GPIO_VIN1_2	<>	3.3[V] *2	IO Expander-10 bit5	No used

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description
25	GPIO_VIN1_3	<>	3.3[V] *2	IO Expander-10 bit6	No used
15	VA_GPIO_18	-	3.3[V]	IO Expander-2 bit1	No used
14	VA_GPIO_19	-	-	IO Expander-2 bit2	No used
13	VA_GPIO_20	-	-	IO Expander-2 bit3	No used
12	VA_GPIO_21	-	-	IO Expander-2 bit4	No used
19	SERIF_VIN1_0	-	-	No used	-
18	SERIF_VIN1_1	-	-	No used	-
17	SERIF_VIN1_2	<>	3.3[V] *2	IO Expander-10 bit7	No used
16	SERIF_VIN1_3	<>	3.3[V] *2	IO Expander-11 bit0	No used
10	I2S_VOUT1_VIN1_DATA	-	-	No used	-
9	I2S_VOUT1_VIN1_LRCLK	-	-	No used	-
8	I2S_VOUT1_VIN1_BCLK	-	-	No used	-
36	I2S_VOUT2_VIN2_MCLK	-	-	No used	-
30	BOARD_VIN1_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_3" pin, Pull-up	VideoIn1 Board ID bit0
29	BOARD_VIN1_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_4" pin, Pull-up	VideoIn1 Board ID bit1
6	BOARD_VIN1_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_5" pin, Pull-up	VideoIn1 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND
50	GND	-	GND	GND	GND
49	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description
38	GND	-	GND	GND	GND
37	GND	-	GND	GND	GND
5	CVBS_IN_M	-	-	NC	-
35	CVBS_IN_P	-	-	NC	-

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control Board

1.3.4. VideoIn1 Board Interface (Standard Reference Hardware)

Figure 6 shows a schematic of Control Board with VIN1 CN that connects to VideoIn1 Board in Standard Reference Hardware. Pin assignments of the connector (VIN1 CN) and connected terminals are listed on Table 1Table 5. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

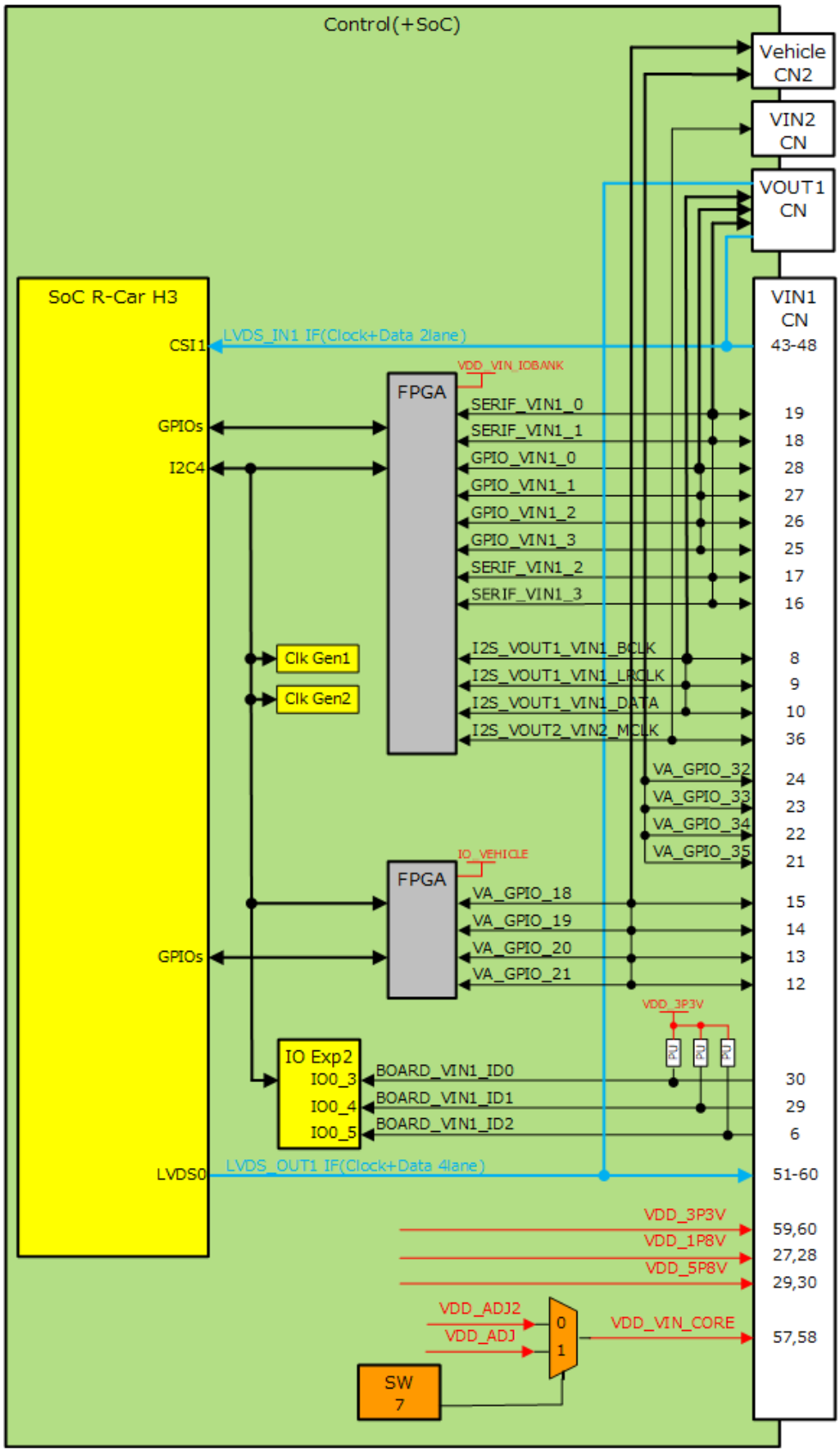


Figure 6 Connectivity between VideoIn1 Board and Control Board (Standard Reference Hardware)

Table 5 Connector (VIN1 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description Example of use
60	LVDS_OUT1_CLK_P	>	LVDS	SoC VideoOut LVDS ch1 Clock+	SoC VideoOut LVDS ch1 Clock+
59	LVDS_OUT1_CLK_M	>	LVDS	SoC VideoOut LVDS ch1 Clock-	SoC VideoOut LVDS ch1 Clock-
58	LVDS_OUT1_LN0_P	>	LVDS	SoC VideoOut LVDS ch1 Data0+	SoC VideoOut LVDS ch1 Data0+
57	LVDS_OUT1_LN0_M	>	LVDS	SoC VideoOut LVDS ch1 Data0-	SoC VideoOut LVDS ch1 Data0-
56	LVDS_OUT1_LN1_P	>	LVDS	SoC VideoOut LVDS ch1 Data1+	SoC VideoOut LVDS ch1 Data1+
55	LVDS_OUT1_LN1_M	>	LVDS	SoC VideoOut LVDS ch1 Data1-	SoC VideoOut LVDS ch1 Data1-
54	LVDS_OUT1_LN2_P	>	LVDS	SoC VideoOut LVDS ch1 Data2+	SoC VideoOut LVDS ch1 Data2+
53	LVDS_OUT1_LN2_M	>	LVDS	SoC VideoOut LVDS ch1 Data2-	SoC VideoOut LVDS ch1 Data2-
52	LVDS_OUT1_LN3_P	>	LVDS	SoC VideoOut LVDS ch1 Data3+	SoC VideoOut LVDS ch1 Data3+
51	LVDS_OUT1_LN3_M	>	LVDS	SoC VideoOut LVDS ch1 Data3-	SoC VideoOut LVDS ch1 Data3-
48	LVDS_IN1_CLK_P *2	<	LVDS	SoC VideoIn LVDS ch1 Clock+	SoC VideoIn LVDS ch1 Clock+
47	LVDS_IN1_CLK_M *2	<	LVDS	SoC VideoIn LVDS ch1 Clock-	SoC VideoIn LVDS ch1 Clock-
46	LVDS_IN1_LN0_P *2	<	LVDS	SoC VideoIn LVDS ch1 Data0+	SoC VideoIn LVDS ch1 Data0+
45	LVDS_IN1_LN0_M *2	<	LVDS	SoC VideoIn LVDS ch1 Data0-	SoC VideoIn LVDS ch1 Data0-
44	LVDS_IN1_LN1_P *2	<	LVDS	SoC VideoIn LVDS ch1 Data1+	SoC VideoIn LVDS ch1 Data1+
43	LVDS_IN1_LN1_M *2	<	LVDS	SoC VideoIn LVDS ch1 Data1-	SoC VideoIn LVDS ch1 Data1-
42	LVDS_IN1_LN2_P *2	<	LVDS	SoC VideoIn LVDS ch1 Data2+	SoC VideoIn LVDS ch1 Data2+
41	LVDS_IN1_LN2_M *2	<	LVDS	SoC VideoIn LVDS ch1 Data2-	SoC VideoIn LVDS ch1 Data2-
40	LVDS_IN1_LN3_P *2	<	LVDS	SoC VideoIn LVDS ch1 Data3+	SoC VideoIn LVDS ch1 Data3+
39	LVDS_IN1_LN3_M *2	<	LVDS	SoC VideoIn LVDS ch1 Data3-	SoC VideoIn LVDS ch1 Data3-
24	VA_GPIO_32	<>	IO_VEHICLE	Vehicle CN1 29pin	GPIO
23	VA_GPIO_33	<>	IO_VEHICLE	Vehicle CN1 28pin	GPIO
22	VA_GPIO_34	<>	IO_VEHICLE	Vehicle CN1 27pin	GPIO
21	VA_GPIO_35	<>	IO_VEHICLE	Vehicle CN1 26pin	GPIO
28	GPIO_VIN1_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Reset
27	GPIO_VIN1_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt
26	GPIO_VIN1_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Enable
25	GPIO_VIN1_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description Example of use
15	VA_GPIO_18	<>	IO_VEHICLE	Vehicle CN1 45pin, FPGA	GPIO
14	VA_GPIO_19	<>	IO_VEHICLE	Vehicle CN1 44pin, FPGA	GPIO
13	VA_GPIO_20	<>	IO_VEHICLE	Vehicle CN1 42pin, FPGA	GPIO
12	VA_GPIO_21	<>	IO_VEHICLE	Vehicle CN1 41pin, FPGA	GPIO
19	SERIF_VIN1_0 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
18	SERIF_VIN1_1 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
17	SERIF_VIN1_2 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
16	SERIF_VIN1_3 *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
10	I2S_VOUT1_VIN1_DATA *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Data
9	I2S_VOUT1_VIN1_LRCLK *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S LR Clock
8	I2S_VOUT1_VIN1_BCLK *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Bit Clock
36	I2S_VOUT2_VIN2_MCLK *3	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Master Clock
30	BOARD_VIN1_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_3" pin, Pull-up	VideoIn1 Board ID bit0
29	BOARD_VIN1_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_4" pin, Pull-up	VideoIn1 Board ID bit1
6	BOARD_VIN1_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_5" pin, Pull-up	VideoIn1 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND
50	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN1	Voltage	Connection of the control board	Description Example of use
49	GND	-	GND	GND	GND
38	GND	-	GND	GND	GND
37	GND	-	GND	GND	GND
5	CVBS_IN_M	<	-	SoC CN1 206pin	No used(CVBS In-)
35	CVBS_IN_P	<	-	SoC CN1 207pin	No used(CVBS In+)

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board
*2: The signal is connected to VideoOut1as well. If used on VideoOut1 Board, output conflict should be avoided.
*3: The signal is connected to VideoIn2 as well. If used on VideoIn2 Board, output conflict should be avoided.

1.3.5. VideoIn2 Board Interface (R-Car H3 Reference Hardware)

Figure 7 shows a schematic illustrating simplified connections between Control Board and VideoIn2 Board in R-Car H3 Reference Hardware. Connector (VIN2 CN) pin assignments and connected terminals are listed on Table 6.

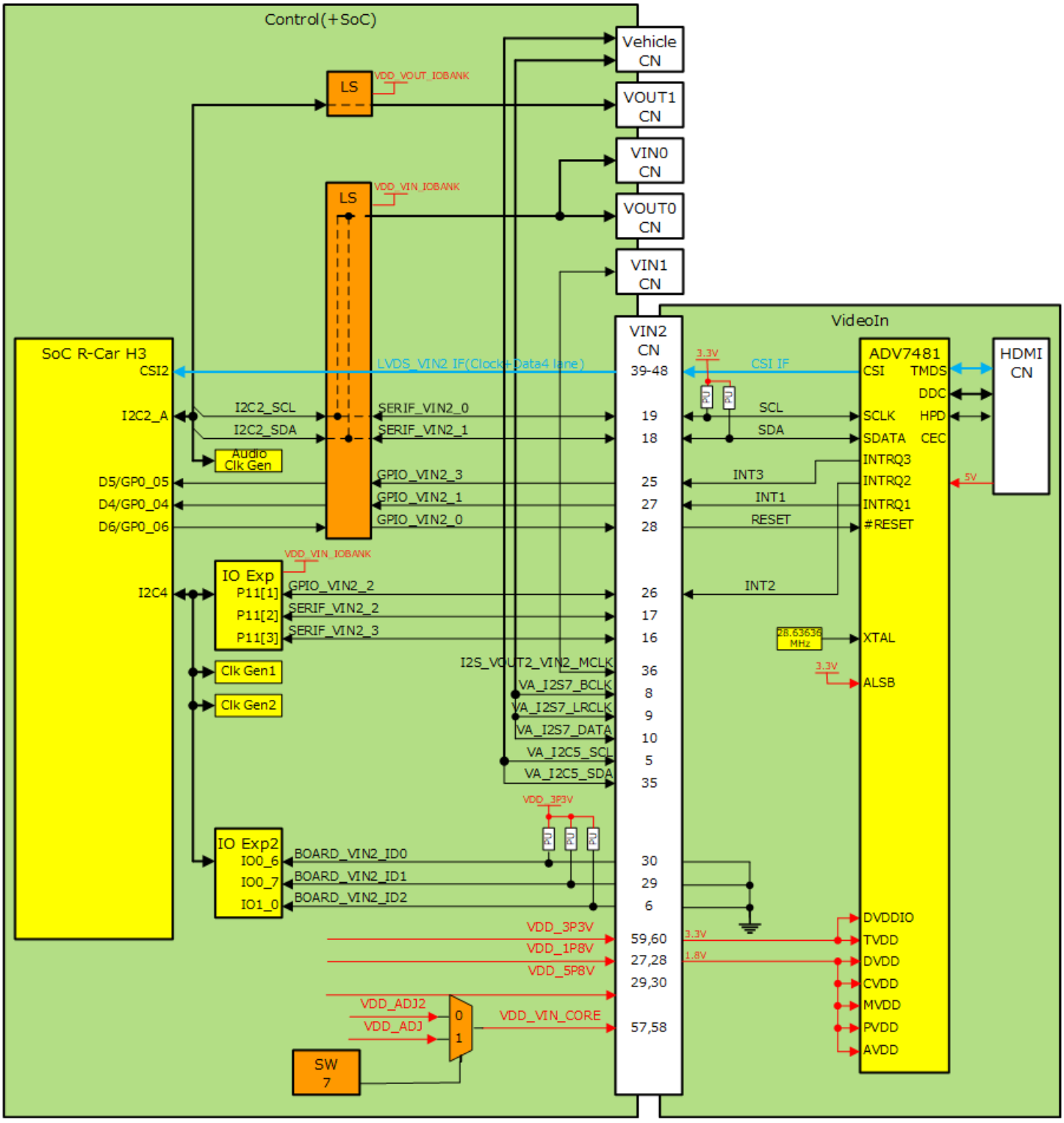


Figure 7 Connectivity between VideoIn2 Board and Control Board (R-Car H3 Reference Hardware)

Table 6 Connector (VIN2 CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description
60	-	-	-	NC	-
59	-	-	-	NC	-
58	-	-	-	NC	-
57	-	-	-	NC	-
56	-	-	-	NC	-
55	-	-	-	NC	-
54	-	-	-	NC	-
53	-	-	-	NC	-
52	-	-	-	NC	-
51	-	-	-	NC	-
48	LVDS_IN2_CLK_P	<	LVDS	R-Car H3 "CSI2_CLKP" pin	CSI ch2 Clock+ (HDMI In to CSI Bridge)
47	LVDS_IN2_CLK_M	<	LVDS	R-Car H3 "CSI2_CLKN" pin	CSI ch2 Clock- (HDMI In to CSI Bridge)
46	LVDS_IN2_LN0_P	<	LVDS	R-Car H3 "CSI2_DATAP0" pin	CSI ch2 Data0+ (HDMI In to CSI Bridge)
45	LVDS_IN2_LN0_M	<	LVDS	R-Car H3 "CSI2_DATAN0" pin	CSI ch2 Data0- (HDMI In to CSI Bridge)
44	LVDS_IN2_LN1_P	<	LVDS	R-Car H3 "CSI2_DATAP1" pin	CSI ch2 Data1+ (HDMI In to CSI Bridge)
43	LVDS_IN2_LN1_M	<	LVDS	R-Car H3 "CSI2_DATAN1" pin	CSI ch2 Data1- (HDMI In to CSI Bridge)
42	LVDS_IN2_LN2_P	<	LVDS	R-Car H3 "CSI2_DATAP2" pin	CSI ch2 Data2+ (HDMI In to CSI Bridge)
41	LVDS_IN2_LN2_M	<	LVDS	R-Car H3 "CSI2_DATAN2" pin	CSI ch2 Data2- (HDMI In to CSI Bridge)
40	LVDS_IN2_LN3_P	<	LVDS	R-Car H3 "CSI2_DATAP3" pin	CSI ch2 Data3+ (HDMI In to CSI Bridge)
39	LVDS_IN2_LN3_M	<	LVDS	R-Car H3 "CSI2_DATAN3" pin	CSI ch2 Data3- (HDMI In to CSI Bridge)
24	-	-	-	NC	-
23	-	-	-	NC	-
22	-	-	-	NC	-
21	-	-	-	NC	-
28	GPIO_VIN2_0	>	3.3[V] *2	R-Car H3 "D6/GP0_06" pin	HDMI In to CSI Bridge Reset
27	GPIO_VIN2_1	<	3.3[V] *2	R-Car H3 "D4/GP0_04" pin	HDMI In to CSI Bridge INTRQ1
26	GPIO_VIN2_2	<>	3.3[V] *2	IO Expander-11 bit1	No used

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description
25	GPIO_VIN2_3	<	3.3[V] *2	R-Car H3 "D5/GP0_05" pin	HDMI In to CSI Bridge INTRQ3
15	-	-	-	NC	-
14	-	-	-	NC	-
13	-	-	-	NC	-
12	-	-	-	NC	-
19	SERIF_VIN2_0	<>	3.3[V] *2	R-Car H3 "RTS0#/SCL2_A" pin	HDMI In to CSI Bridge SCLK
18	SERIF_VIN2_1	<>	3.3[V] *2	R-Car H3 "SCK0/SDA2_A" pin	HDMI In to CSI Bridge SDATA
17	SERIF_VIN2_2	<>	3.3[V] *2	IO Expander-11 bit2	No used
16	SERIF_VIN2_3	<>	3.3[V] *2	IO Expander-11 bit3	No used
10	VA_I2S7_DATA	-	-	No used	-
9	VA_I2S7_LRCLK	-	-	No used	-
8	VA_I2S7_BCLK	-	-	No used	-
36	I2S_VOUT2_VIN2_MCLK	-	-	No used	-
30	BOARD_VIN2_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_6" pin, Pull-up	VideoIn2 Board ID bit0
29	BOARD_VIN2_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_7" pin, Pull-up	VideoIn2 Board ID bit1
6	BOARD_VIN2_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO1_0" pin, Pull-up	VideoIn2 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND
50	GND	-	GND	GND	GND
49	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description
38	GND	-	GND	GND	GND
37	GND	-	GND	GND	GND
5	VA_I2C5_SCL	<>	3.3[V]	R-Car H3 "AVB_AVTP_MATCH_A/SCL5" pin, Pull-up, Audio Codec(AK4613VQ) SCL/CCLKpin	No used
35	VA_I2C5_SDA	<>	3.3[V]	R-Car H3 "AVB_AVTP_CAPTURE_A/SDA5" pin, Pull-up, Audio Codec(AK4613VQ) SDA/CDTIpin	No used

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA VIN IO voltage) on Control Board

1.3.6. VideoIn2 Board Interface (Standard Reference Hardware)

Figure 8 shows a schematic of Control Board with VIN2 CN that connects to VideoIn2 Board in Standard Reference Hardware. Pin assignments of the connector (VIN2 CN) and connected terminals are listed on Table 7. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

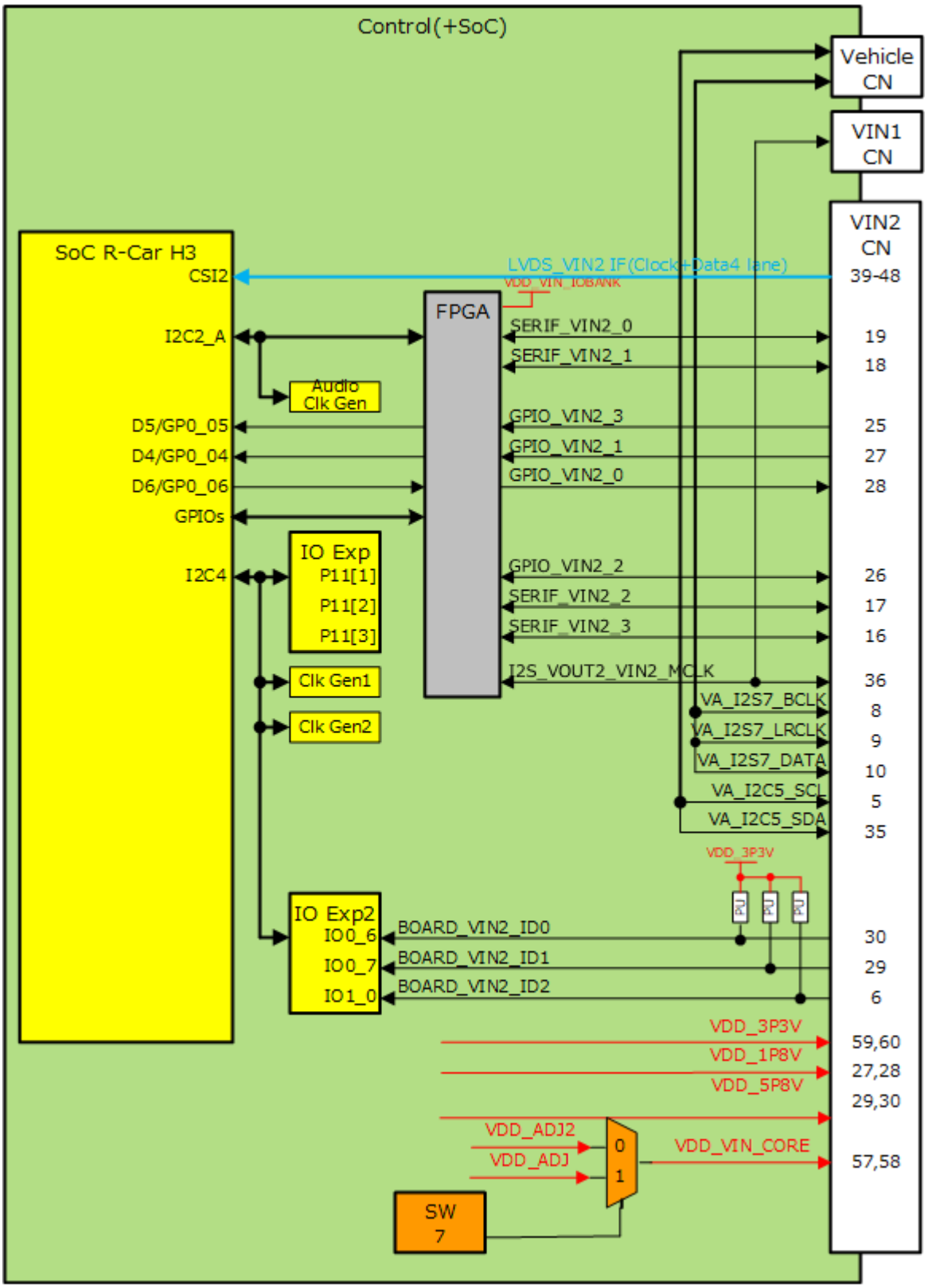


Figure 8 Connectivity between VideoIn2 Board and Control Board (Standard Reference Hardware)

Table 7 Connector (VIN2 CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description Example of use
60	-	-	-	NC	-
59	-	-	-	NC	-
58	-	-	-	NC	-
57	-	-	-	NC	-
56	-	-	-	NC	-
55	-	-	-	NC	-
54	-	-	-	NC	-
53	-	-	-	NC	-
52	-	-	-	NC	-
51	-	-	-	NC	-
48	LVDS_IN2_CLK_P	<	LVDS	SoC VideoIn LVDS ch2 Clock+	SoC VideoIn LVDS ch2 Clock+
47	LVDS_IN2_CLK_M	<	LVDS	SoC VideoIn LVDS ch2 Clock-	SoC VideoIn LVDS ch2 Clock-
46	LVDS_IN2_LN0_P	<	LVDS	SoC VideoIn LVDS ch2 Data0+	SoC VideoIn LVDS ch2 Data0+
45	LVDS_IN2_LN0_M	<	LVDS	SoC VideoIn LVDS ch2 Data0-	SoC VideoIn LVDS ch2 Data0-
44	LVDS_IN2_LN1_P	<	LVDS	SoC VideoIn LVDS ch2 Data1+	SoC VideoIn LVDS ch2 Data1+
43	LVDS_IN2_LN1_M	<	LVDS	SoC VideoIn LVDS ch2 Data1-	SoC VideoIn LVDS ch2 Data1-
42	LVDS_IN2_LN2_P	<	LVDS	SoC VideoIn LVDS ch2 Data2+	SoC VideoIn LVDS ch2 Data2+
41	LVDS_IN2_LN2_M	<	LVDS	SoC VideoIn LVDS ch2 Data2-	SoC VideoIn LVDS ch2 Data2-
40	LVDS_IN2_LN3_P	<	LVDS	SoC VideoIn LVDS ch2 Data3+	SoC VideoIn LVDS ch2 Data3+
39	LVDS_IN2_LN3_M	<	LVDS	SoC VideoIn LVDS ch2 Data3-	SoC VideoIn LVDS ch2 Data3-
24	-	-	-	NC	-
23	-	-	-	NC	-
22	-	-	-	NC	-
21	-	-	-	NC	-
28	GPIO_VIN2_0	>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Reset
27	GPIO_VIN2_1	<	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt
26	GPIO_VIN2_2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Enable

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description Example of use
25	GPIO_VIN2_3	<	VDD_VIN_IOBANK	FPGA	GPIO, e.g. Interrupt
15	-	-	-	NC	-
14	-	-	-	NC	-
13	-	-	-	NC	-
12	-	-	-	NC	-
19	SERIF_VIN2_0	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SCL/SPI Clock/UART SoC RTS
18	SERIF_VIN2_1	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI CS/UART SoC CTS
17	SERIF_VIN2_2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataOut/UART SoC RxD
16	SERIF_VIN2_3	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2C SDA/SPI SoC DataIn/UART SoC TxD
10	VA_I2S7_DATA	<>	IO_AUDIO	Vehicle CN2 86pin	No used, I2S ch7 Data
9	VA_I2S7_LRCLK	<>	IO_AUDIO	Vehicle CN2 87pin	No used, I2S ch7 LR Clock
8	VA_I2S7_BCLK	<>	IO_AUDIO	Vehicle CN2 88pin	No used, I2S ch7 Bit Clock
36	I2S_VOUT2_VIN2_MCLK *2	<>	VDD_VIN_IOBANK	FPGA	GPIO, e.g. I2S Master Clock
30	BOARD_VIN2_ID0	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_6" pin, Pull-up	VideoIn2 Board ID bit0
29	BOARD_VIN2_ID1	<	3.3[V]	IO Expander(PCA9539)-2 "IO0_7" pin, Pull-up	VideoIn2 Board ID bit1
6	BOARD_VIN2_ID2	<	3.3[V]	IO Expander(PCA9539)-2 "IO1_0" pin, Pull-up	VideoIn2 Board ID bit2
4	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
3	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
34	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
33	VDD_VIN_CORE	>	Power:1.5[V] *1	1.2[V] output LDO	Power
32	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
20	GND	-	GND	GND	GND
11	GND	-	GND	GND	GND
7	GND	-	GND	GND	GND

Pin	Signal Name	Direction Control - VIN2	Voltage	Connection of the control board	Description Example of use
50	GND	-	GND	GND	GND
49	GND	-	GND	GND	GND
38	GND	-	GND	GND	GND
37	GND	-	GND	GND	GND
5	VA_I2C5_SCL	<>	3.3[V]	R-Car H3 "AVB_AVTP_MATCH_A/SCL5" pin, Pull-up, Audio Codec(AK4613VQ) SCL/CCLKpin	I2C SCL
35	VA_I2C5_SDA	<>	3.3[V]	R-Car H3 "AVB_AVTP_CAPTURE_A/SDA5" pin, Pull-up, Audio Codec(AK4613VQ) SDA/CDTIpin	I2C SDA

*1: Voltage depends on the power supply switch setting (VIN Core voltage) on Control Board

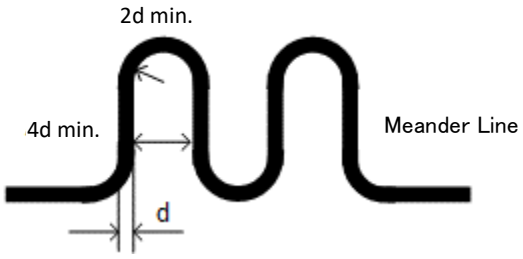
*2: The signal is connected to VideoIn1as well. If used on VideoIn1 Board, output conflict should be avoided.

1.4. Board Layout Consideration

Due to LVDS lines on Control Board, traces on VideoIn Board need to be designed in accordance with the following restrictions:

Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and –) must be 0.1[mm] maximum.
- Difference between an average length of a clock pair (average of + signal and – signal)/a data signal pair： 0.2[mm] maximum.
- Maximum Trace Length: 60[mm]
- Differential impedance：100[Ω](100[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be at least twice the width of the trace. The gap between the meander traces should be at least four times the trace width.



Power Supply

- Comply with power supply requirements (impedance property, etc.) of the device to connect.
  If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[℃] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.

2. Disclaimer

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